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MS-7756

m-ATX

Ver: 1.0(243.84 * 243.84)

H/W:JaysonChen

PM:BobbyYuan

Intel -MahoBay

plamform H77

CPU:

System Chipset:

IVY bridge LGA1155

Panther Point H77

Onboard Chip:

HD Audio Codec:ALC892 colay 887

LAN-RTL8111E colay8105E

SIO:Fintek F71868AD

Flash ROM: SPI 64 MB

Main Memory:

DDRIII (1066/1333/1600MHz) * 4 (Dual Channel)

ACPI:

PWM:

UPI

VRD12 -UT501 3+1 Phase

Expansion Slots:

Other:

PCI Express (X16) Slot * 1

USB2.0 *10

PCI Express (X1) Slot * 2

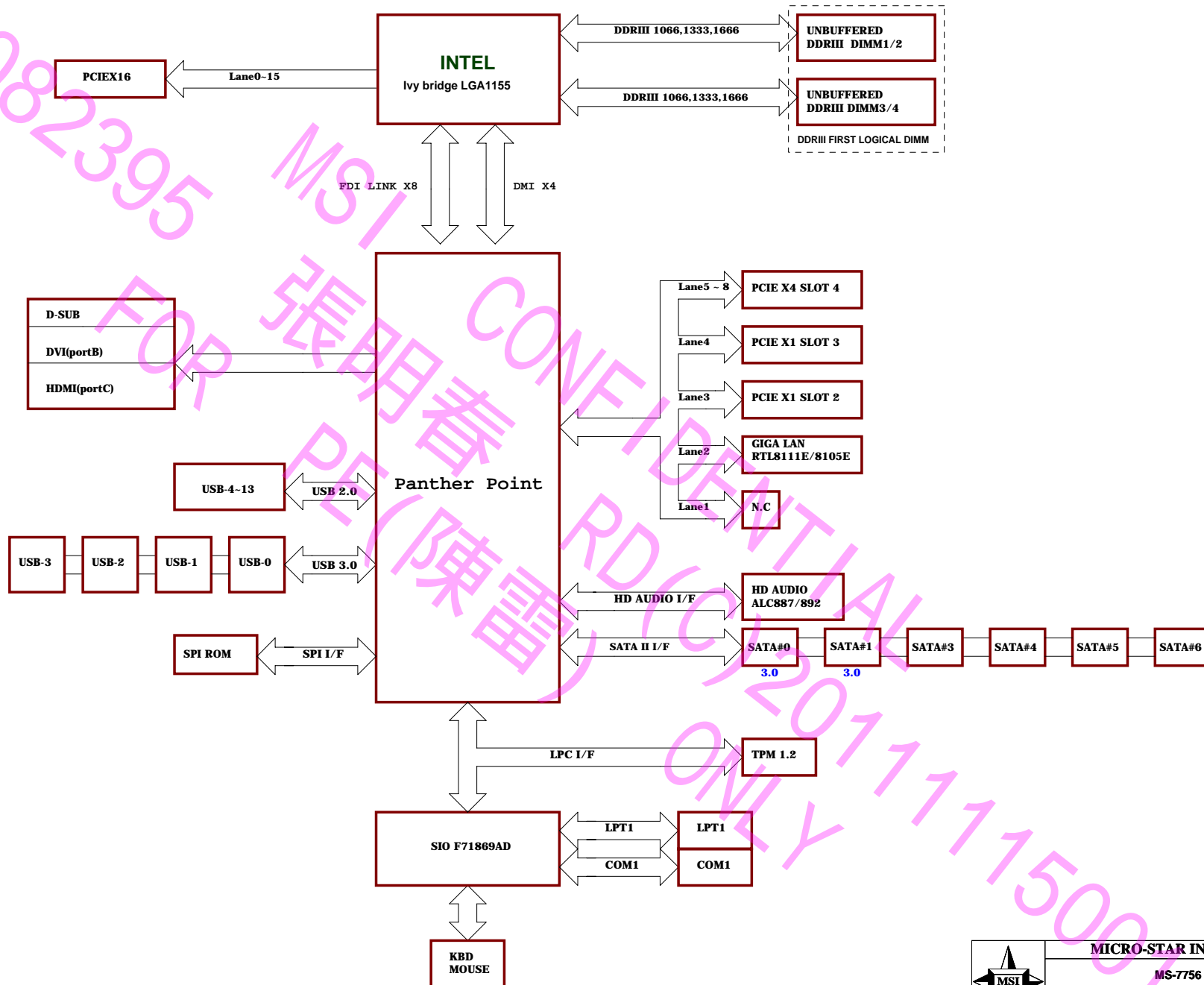
REAL USB3.0 *2

PCI Express (X4) Slot * 1

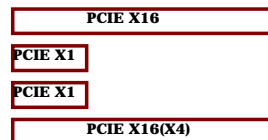
FRONT USB3.0 *2

SATA3.0 x2+SATA2.0 x4 (PCH)

MS-7756 Block Diagram



Slot Sequence:



MICRO-STAR INT'L CO.,LTD

MS-7756

Size Custom	Document Description Block Diagram	Rev 1.0
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CPU1E 5 OF 11

BCLK_0
BCLK#_0VCCP_SELECT
VCCSA_VID

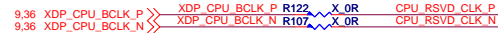
VCCSA_SENSE

VIDCLK
VIDOUT

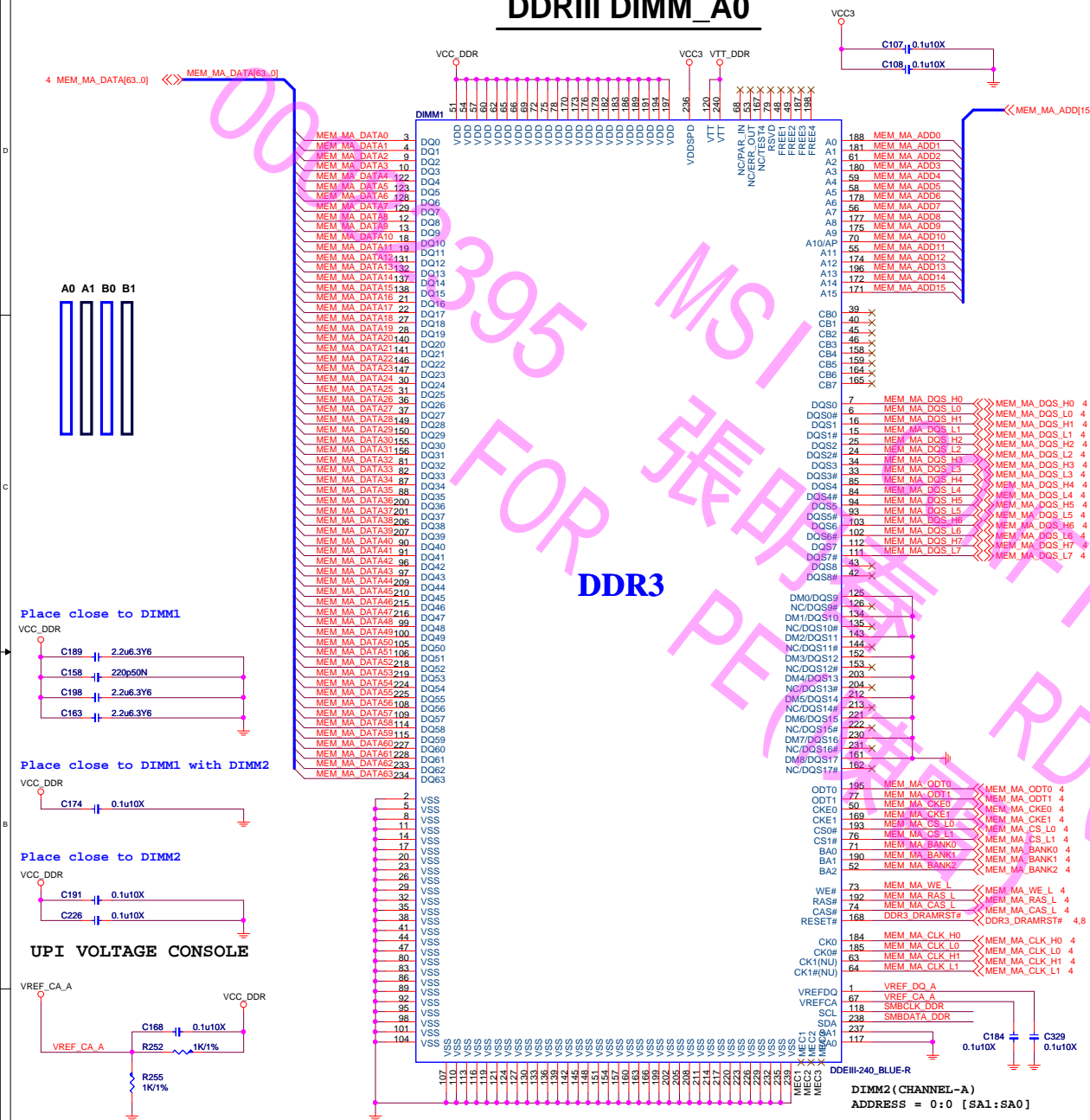
VIDALERT#

VCC_SENSE
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VSSAXG_SENSETDO
TDITCK
TMSTRST#
PRDY#PREQ#
DBR#BPM#_0
BPM#_1BPM#_2
BPM#_3BPM#_4
BPM#_5BPM#_6
BPM#_7CFG_0
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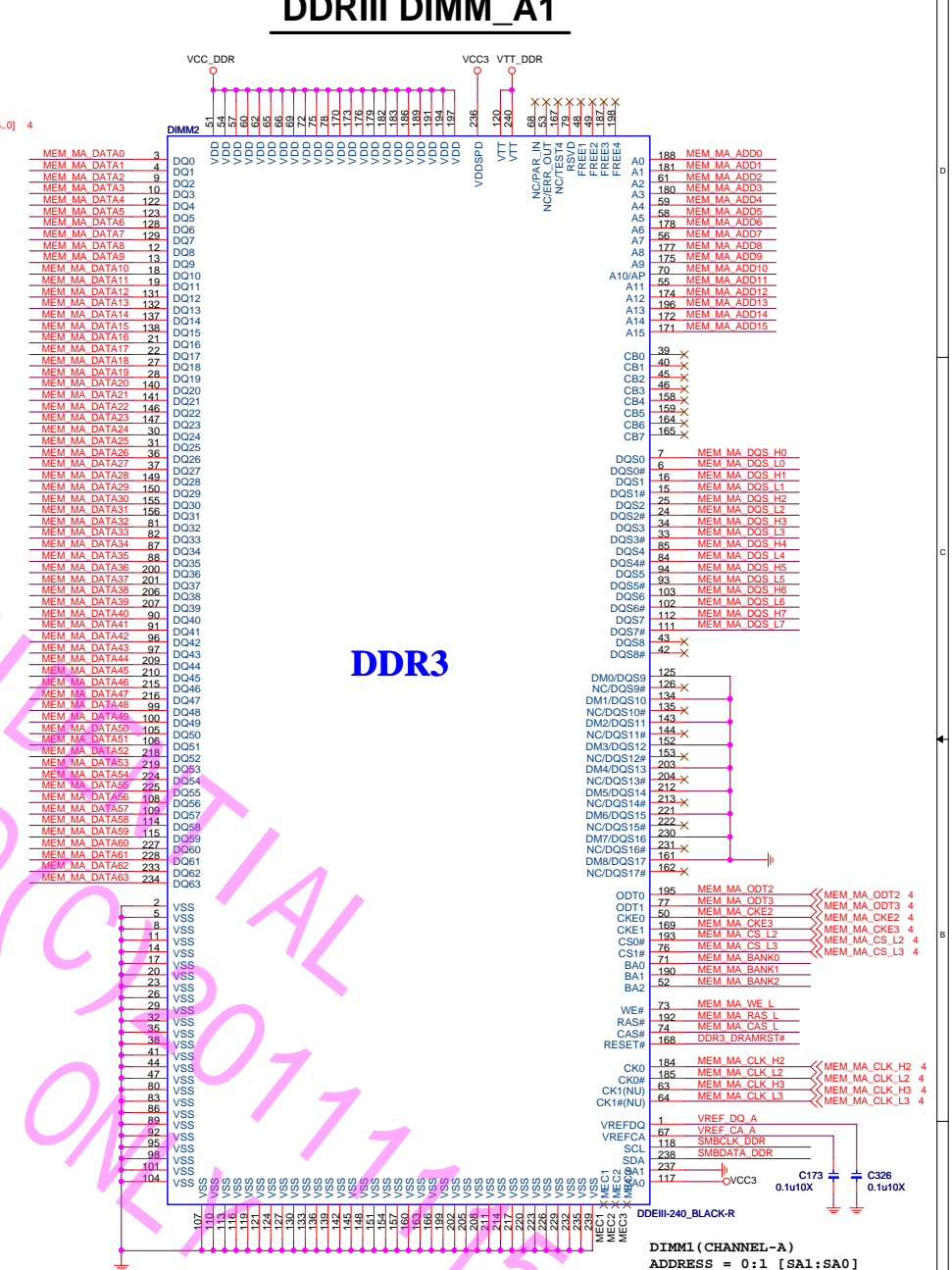




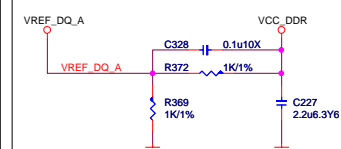
DDRIII DIMM_A0



DDRIII DIMM_A1



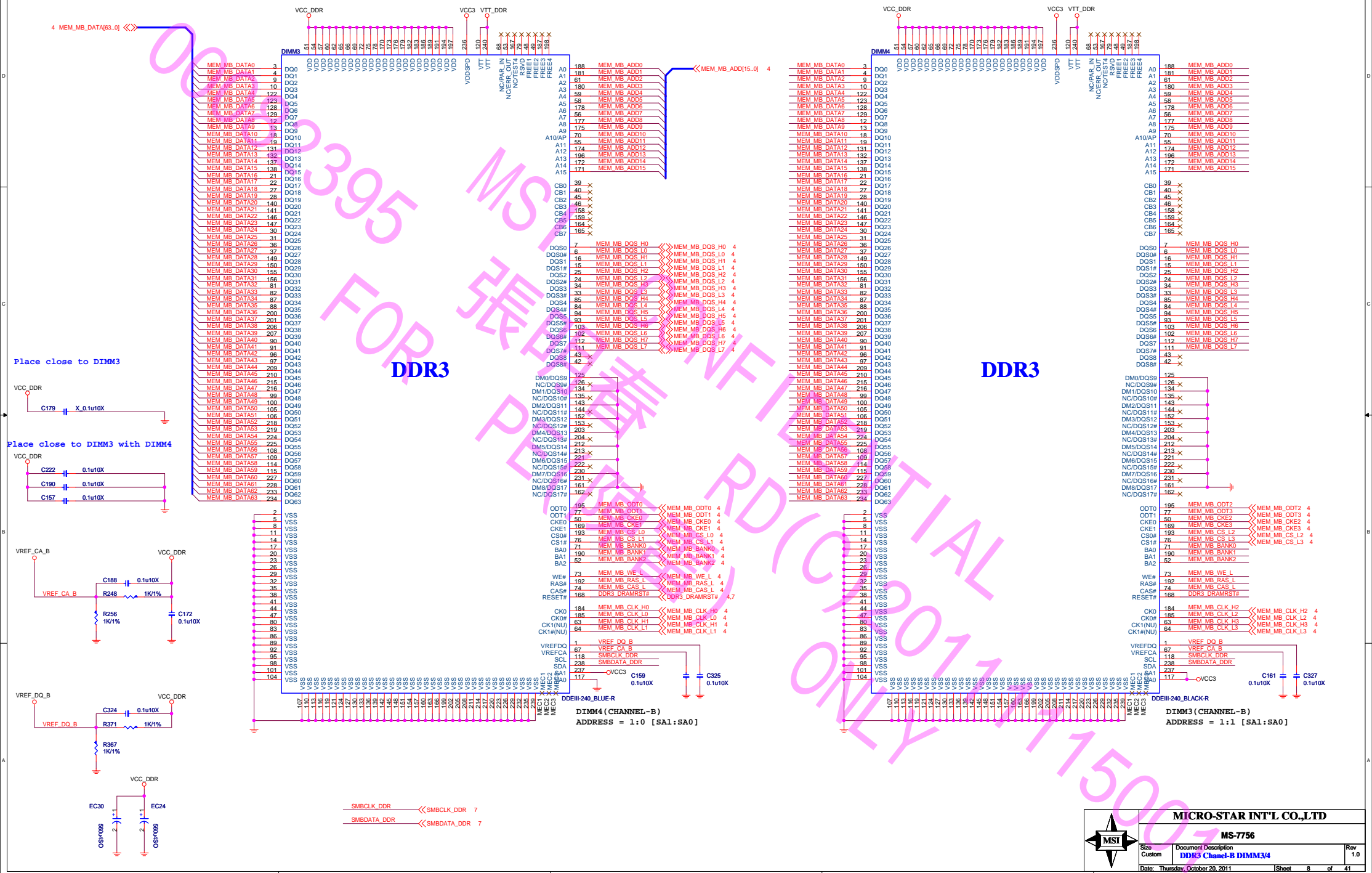
UPI VOLTAGE CONSOLE

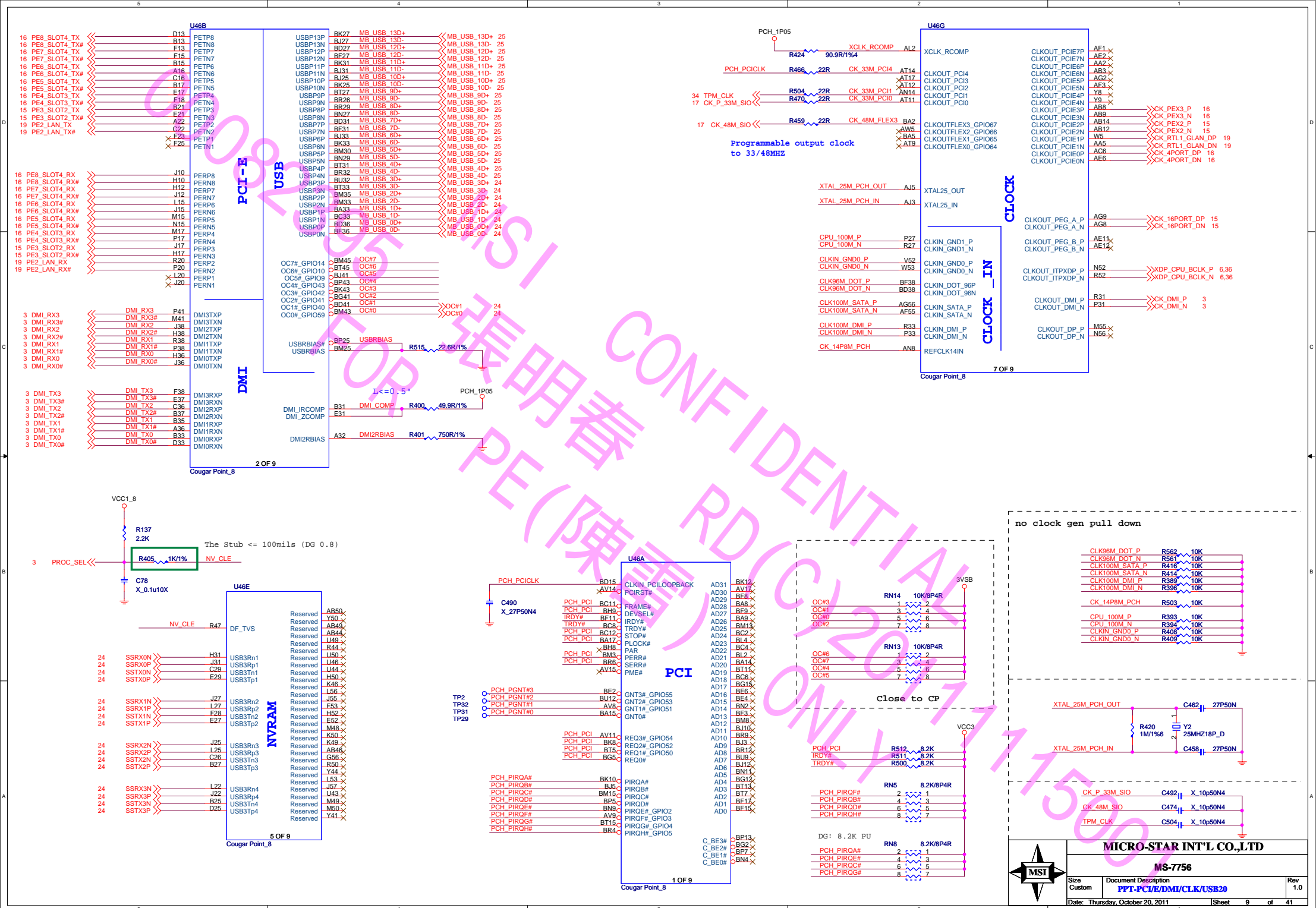


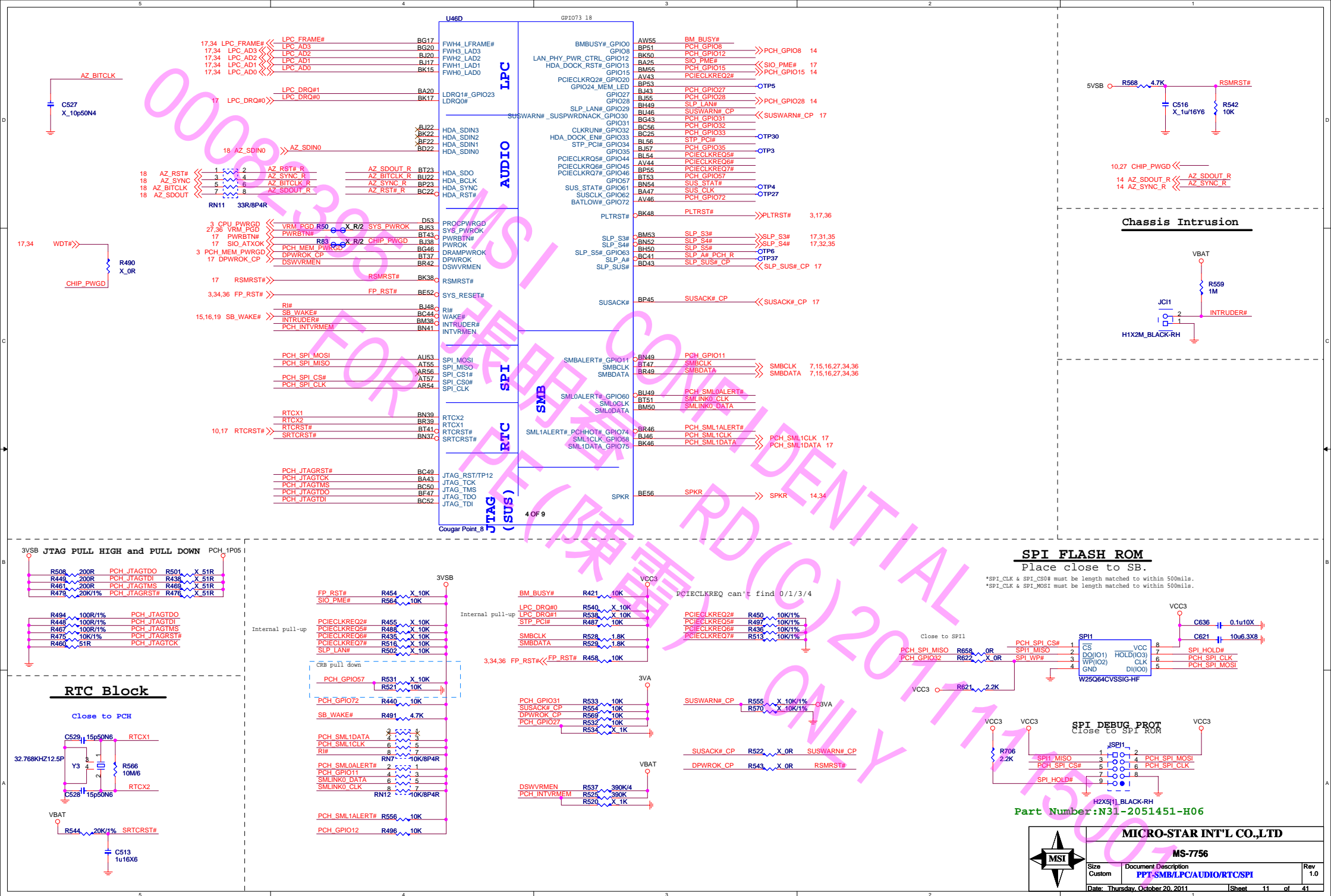
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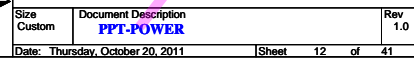
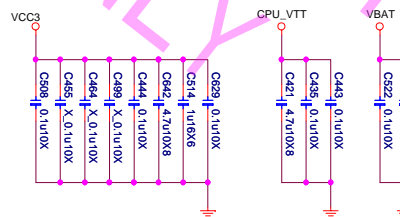
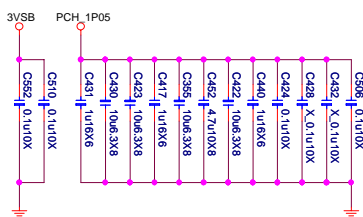
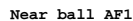
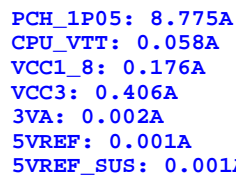
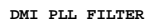
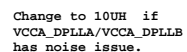
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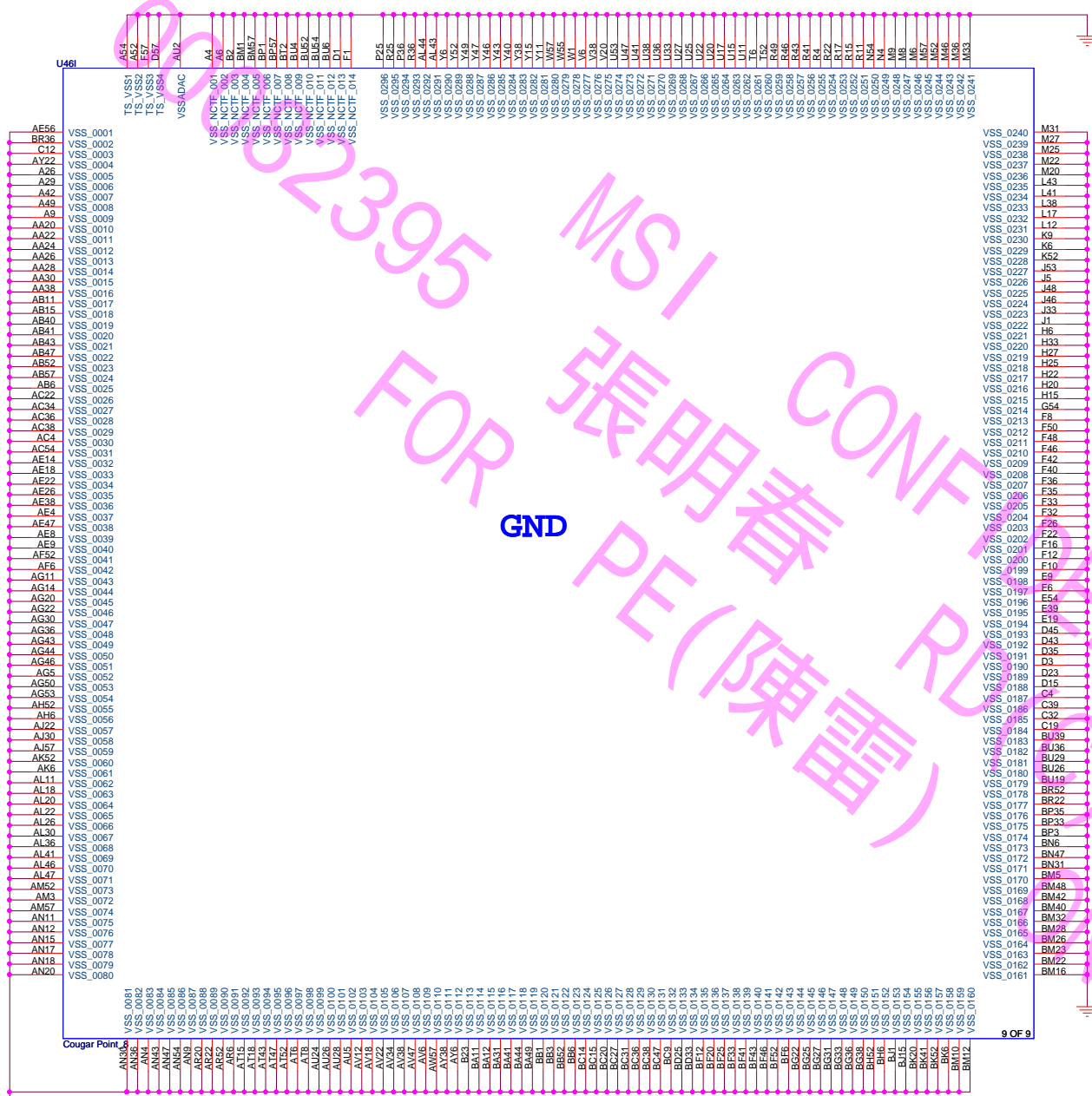
DDRIII DIMM_B1



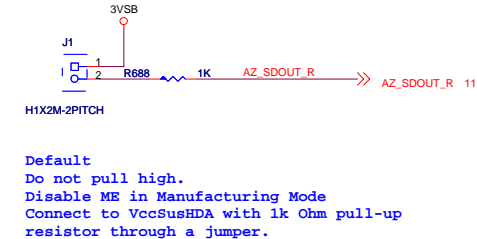
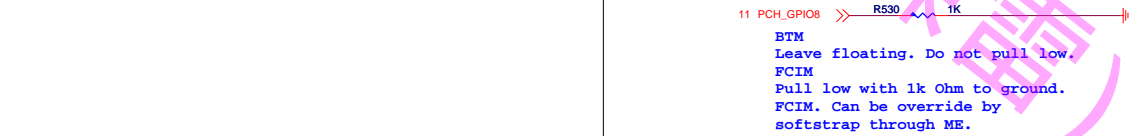
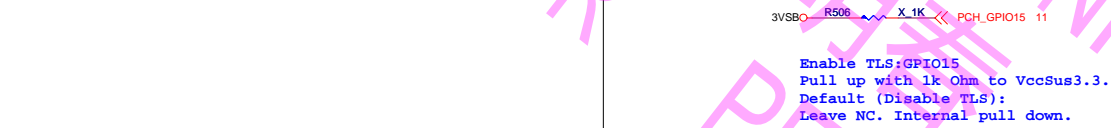
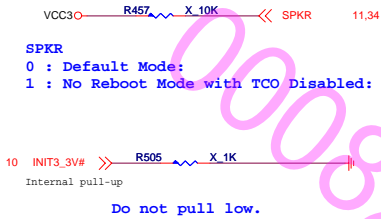








PCH Straps

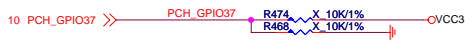


Since Pin has strap functionality that requires internal pull-down to be sampled at rising PWROK, following guidelines are required to be followed:

a) When Used as SATA2GP/SATA3GP for Mechanical Presence detect - Use a weak external pull-up (150K-200K ohms) to Vcc3_3 OR use 10K external pull-up that is enabled only after PLTRST# de-assertion.

b) When Used as GP Input (Pin HW default) - Ensure GPI is not driven high during strap sampling window

When Unused as GPIO or SATA[x]GP - Use 8.2K-10K pull-down to ground.

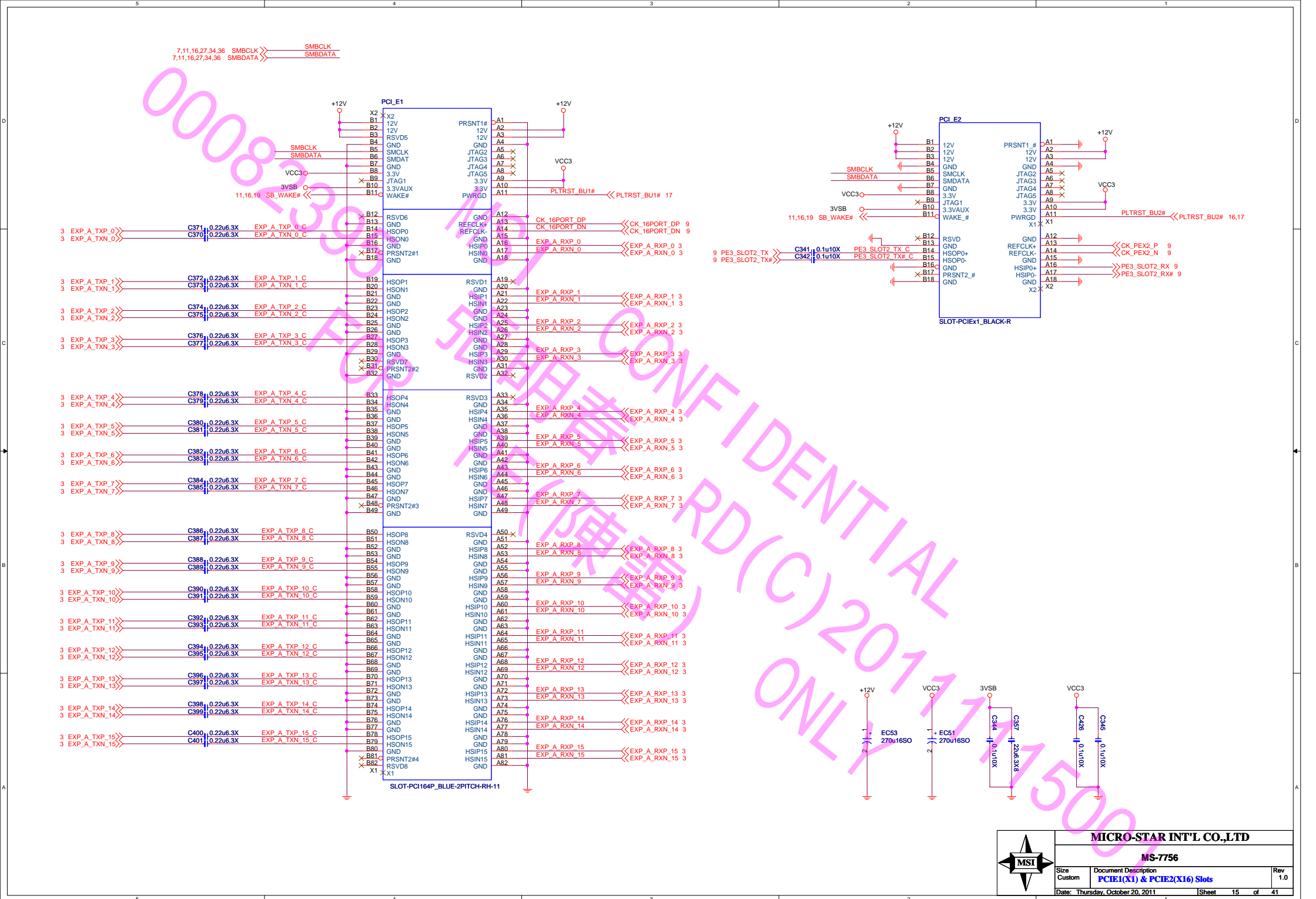


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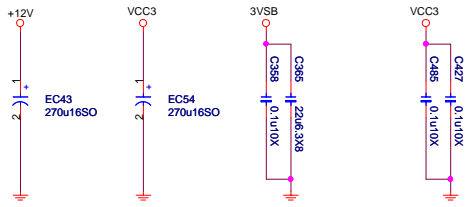
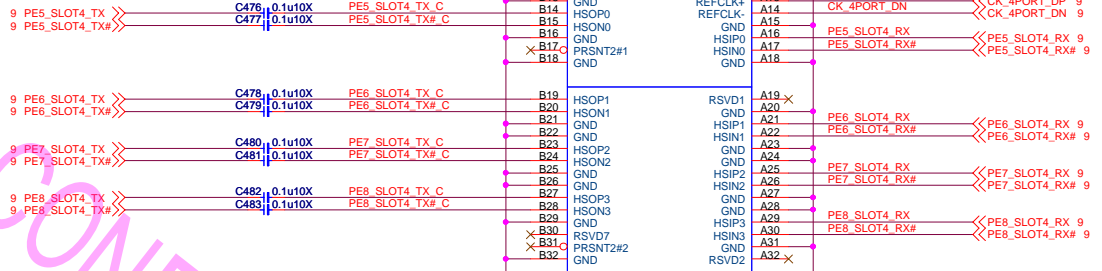
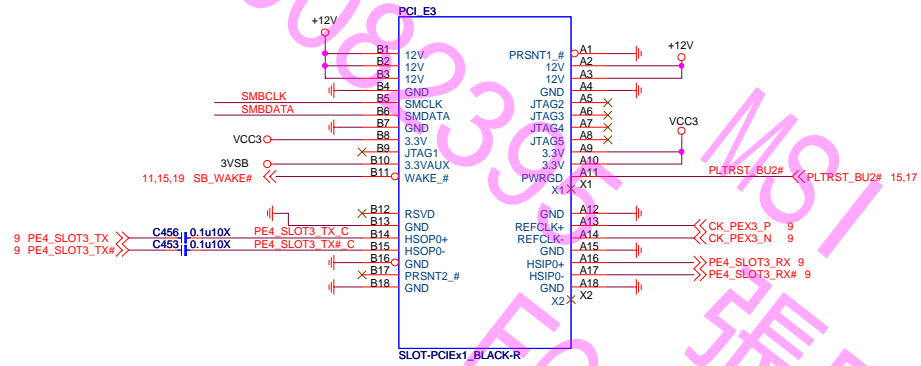
b) When Used as GP Input (Pin HW default) - Ensure GPI is not driven high during strap sampling window

When Unused as GPIO or SATA[x]GP - Use 8.2K-10K pull-down to ground.



7,11,15,27,34,36 SMBCLK
7,11,15,27,34,36 SMBDATA

PCI Express X4 Slot



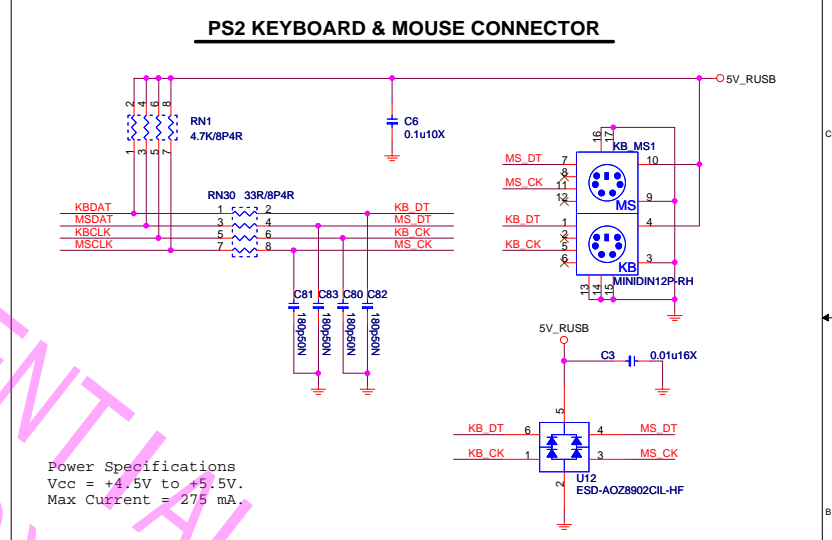
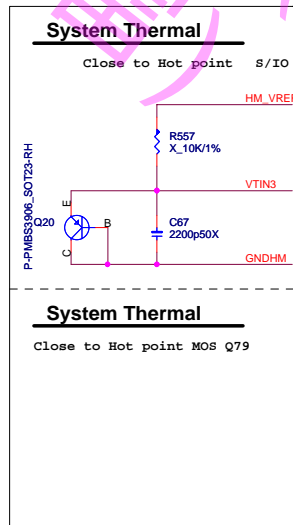


Diagram showing the connections for pins 1 through 10 of the ATmega328P microcontroller:

- SOUTA** (Pin 1) to **R186** (560R) to **X 560R**
- DTRAP#** (Pin 2) to **R184** (560R) to **X 560R**
- STRAP TIMING** (Pin 3) to **R191** (560R) to **X 560R**
- STRAP DPORT** (Pin 4) to **R23** (560R) to **X 560R**
- RTSA#** (Pin 5) to **R183** (560R) to **X 560R**
- PLTRST_BU1#** (Pin 6) to **R39** (820R1%) to **X 820R1%**
- A20GATE** (Pin 7) to **R43** (4.7K) to **X 4.7K**
- WDT#** (Pin 8) to **R12** (10K) to **X 10K**
- SIO TRIP#** (Pin 9) to **R38** (4.7K) to **X 4.7K**
- SIO ATXOK** (Pin 10) to **R71** (4.7K) to **X 4.7K**

OPT BOM

CC3

Component	Value	Function	Component	Value
R138	X 4.7K	SIO_GPIO32	R140	4.7K
R123	X 4.7K	SIO_GPIO33	R119	4.7K
R115	X 4.7K	SIO_GPIO34	R110	4.7K

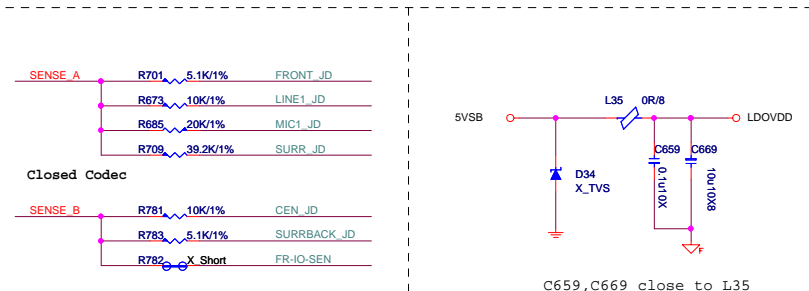
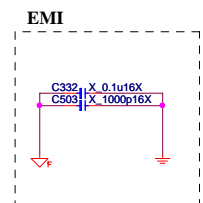
The schematic diagram illustrates the power supply network for the i.MX6UL SoC. It shows the following components and connections:

- VCCPO** is connected to **VIN1** through resistor **R194** (10K/1%). A capacitor **C8** (10u10Y8) is connected to **VIN1** to ground.
- +CPU_GFX** is connected to **VIN2** through resistor **R193** (10K/1%). A capacitor **C87** (X_10u10Y8) is connected to **VIN2** to ground.
- VCC5** is connected to **VIN3** through resistor **R196** (200K/1%). A capacitor **C93** (X_10u10Y8) is connected to **VIN3** to ground. Resistor **R195** (47K/1%) is connected to **VIN3** to ground.
- +12VIN** is connected to **VIN4** through resistor **R192** (200K/1%). A capacitor **C86** (X_100p50N6) is connected to **VIN4** to ground. Resistor **R190** (20K/1%) is connected to **VIN4** to ground.
- VCC_DDR** is connected to **VIN5** through resistor **R195** (10K/1%). A capacitor **C85** (X_0.01u16X) is connected to **VIN5** to ground. Resistor **R179** (10K/1%) is connected to **VIN5** to ground.
- CPU_VTT** is connected to **VIN6** through resistor **R175** (10K/1%). A capacitor **C94** (X_0.01u16X) is connected to **VIN6** to ground.

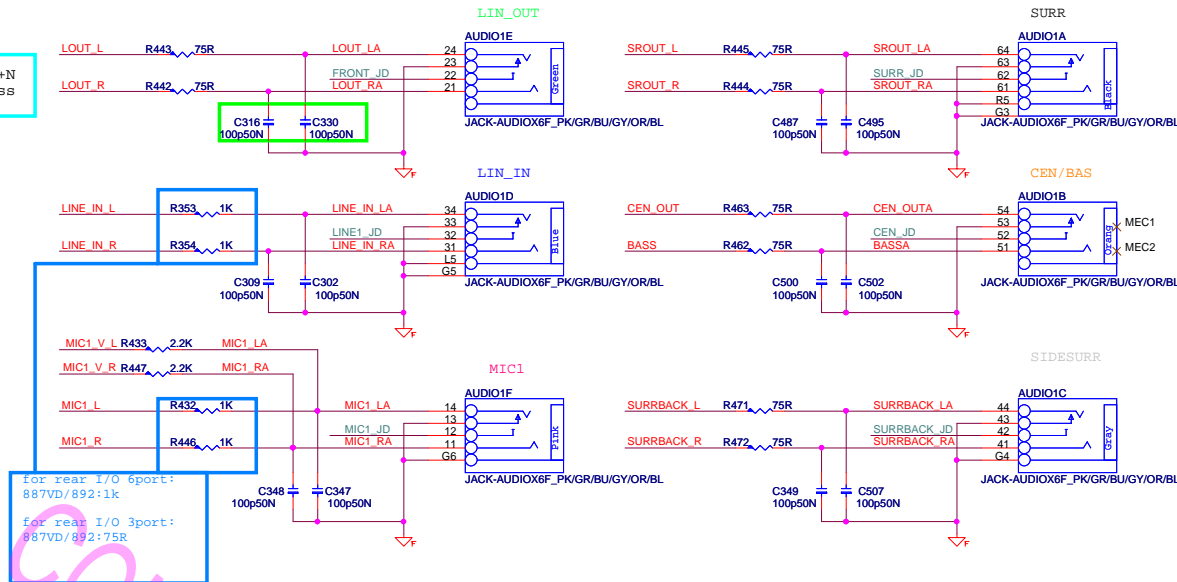


MICRO-STAR INT'L CO.,LTD		
MS-7756		
Size Custom	Document Description SIO-Fintek F71869AD	Rev 1.0

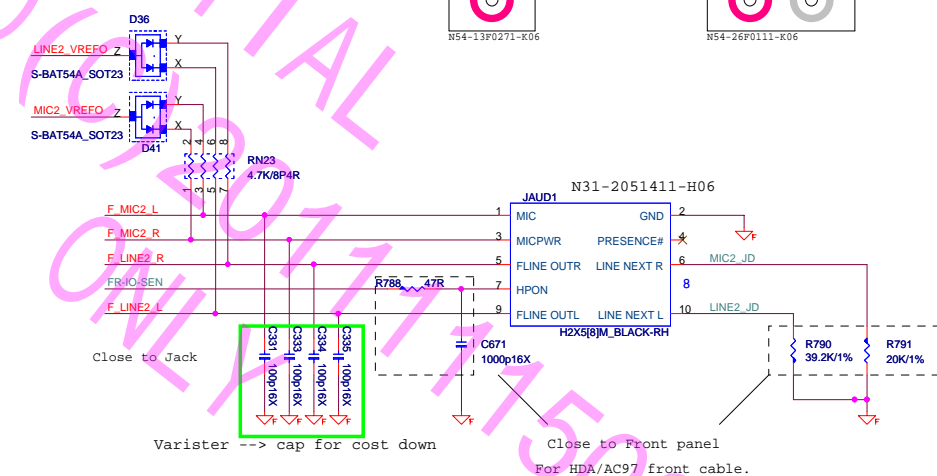
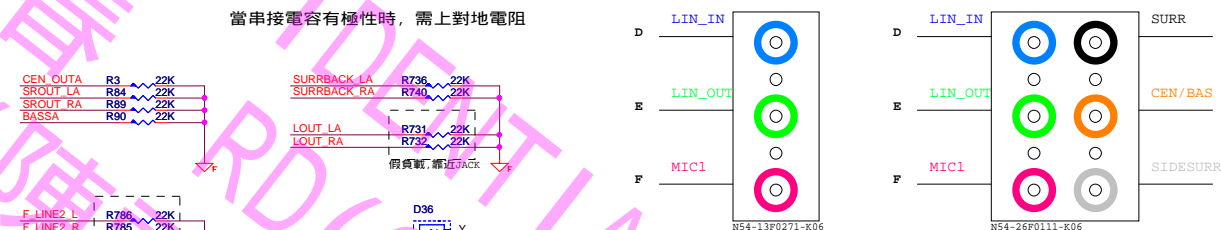
ALC892



用SMD CAP 手動量測會FAIL在THD+N
用EL-CAP or SOLID cap, 才會pass



當串接電容有極性時，需上對地電阻



RN22
75R/8P4R

Pin	Signal
1	MIC2_R
2	F_MIC2_R
3	MIC2_L
4	F_MIC2_L
5	LINE2_L
6	F_LINE2_L
7	LINE2_R
8	F_LINE2_R



MICRO-STAR INT'L CO.,LTD

MS-7756

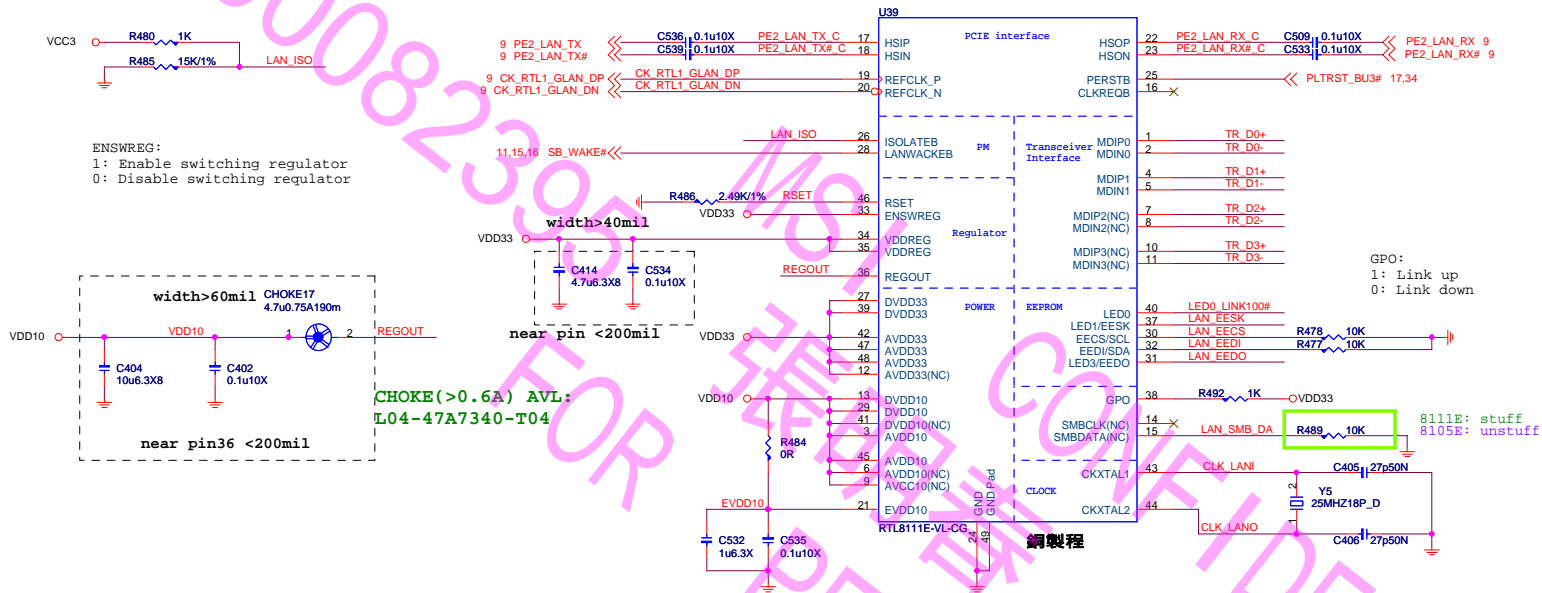
Audio Codec ALC892/887

Rev	1.0
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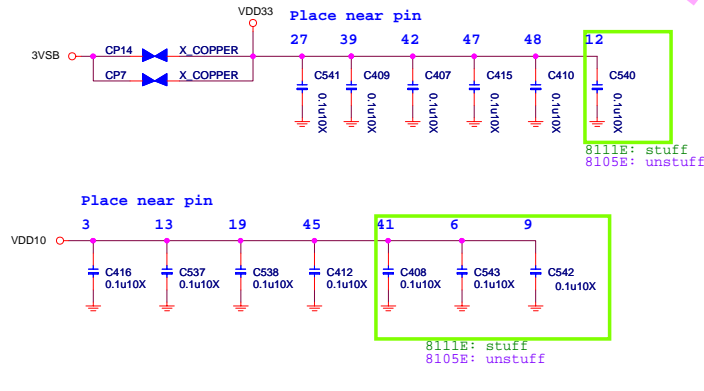
Date: Thursday, October 20, 2011	Sheet 18 of 41
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RTL8111E Giga LAN

RTL8105E 10/100M LAN



3.3v Power on rise time : 1-100ms. MAX: 163mA



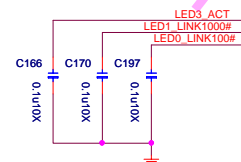
8111E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13

8105E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	14/75	46/248
100 M Idle/TxRx	43/66	142/218
S0 ALDPS	3.2	11

only support LED0+LED1/LED1+LED3 dual color LED combinations when using EEPROM



Giga-Lan	10/100-Lan
N58-22F0731 Link Yellow Active Blinking 1000 Orange 100 Green 10 None	N58-22F0771 Link Yellow Active Blinking 1000 Orange 100 Green 10 None
19 20 21 22	19 20 21 22



MICRO-STAR INT'L CO.,LTD

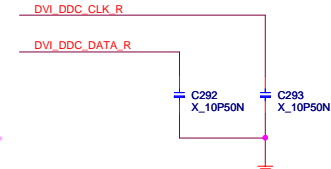
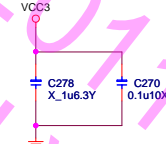
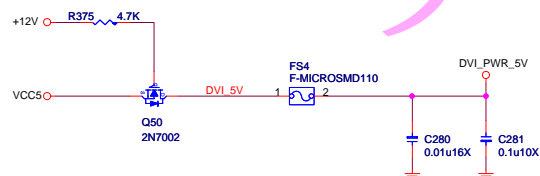
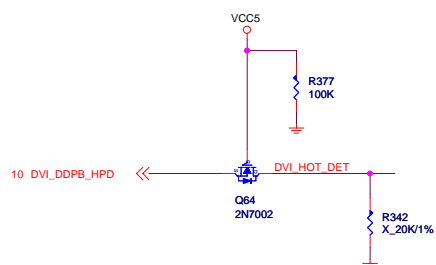
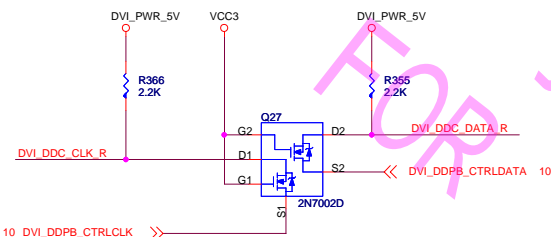
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Size	Document Description	Rev
Custom	LAN-RTL8111E/8105E	1.0

Date: Thursday, October 20, 2011 Sheet 19 of 41

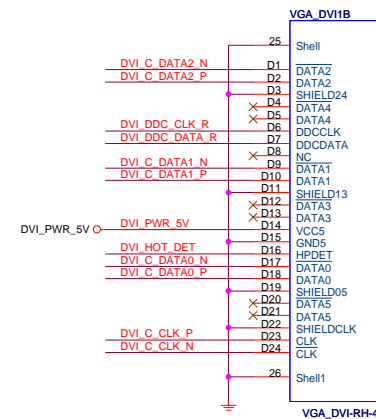
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

10 DVI_DDPB_CLK_N C337 0.1u10X DVI_C_CLK_N R498 680R DVI_DATA_CLK_DN
10 DVI_DDPB_CLK_P C336 0.1u10X DVI_C_CLK_P R524 680R DVI_DATA_CLK_DP
10 DVI_DDPB_TXN0 C362 0.1u10X DVI_C_DATA0_N R493 680R DVI_DATA0_DN
10 DVI_DDPB_TXP0 C361 0.1u10X DVI_C_DATA0_P R507 680R DVI_DATA0_DP
10 DVI_DDPB_TXN1 C336 0.1u10X DVI_C_DATA1_N R519 680R DVI_DATA1_DN
10 DVI_DDPB_TXP1 C339 0.1u10X DVI_C_DATA1_P R523 680R DVI_DATA1_DP
10 DVI_DDPB_TXN2 C364 0.1u10X DVI_C_DATA2_N R526 680R DVI_DATA2_DN
10 DVI_DDPB_TXP2 C363 0.1u10X DVI_C_DATA2_P R514 680R DVI_DATA2_DP



For EMI

DVI_C_DATA0_N R871 220R/1%
DVI_C_DATA0_P R871 220R/1%
DVI_C_DATA1_N R874 220R/1%
DVI_C_DATA1_P R874 220R/1%
DVI_C_CLK_N R873 220R/1%
DVI_C_CLK_P R873 220R/1%
DVI_C_DATA2_N R872 220R/1%
DVI_C_DATA2_P R872 220R/1%



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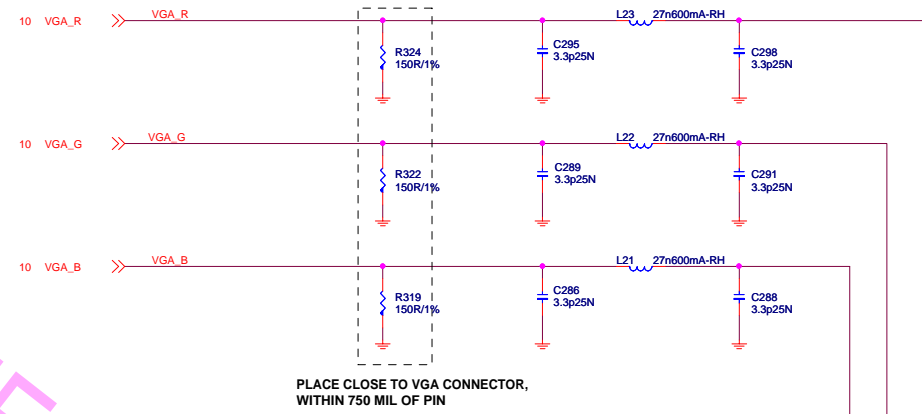
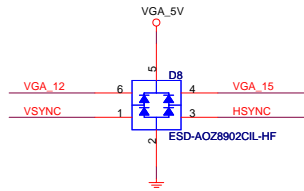
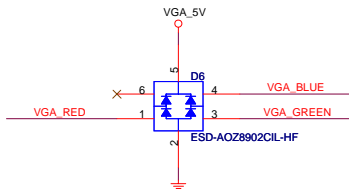
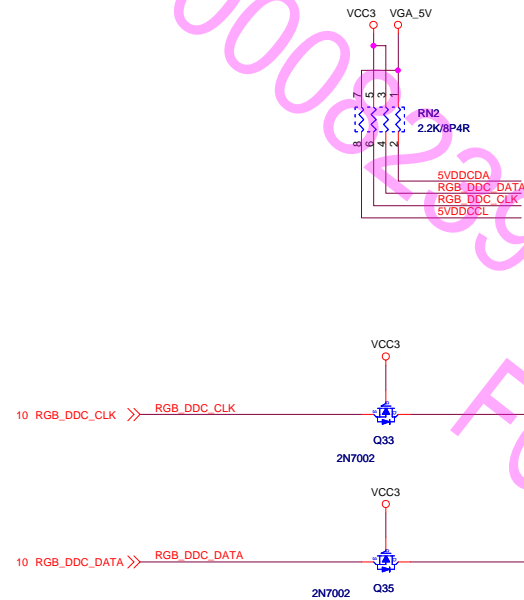
Size	Document Description	Rev
Custom	DVI Connector	1.0
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00082395
MSI
FOR 張明春
PE (陳雷)
RD(C)2011111500
CONFIDENTIAL
ONLY

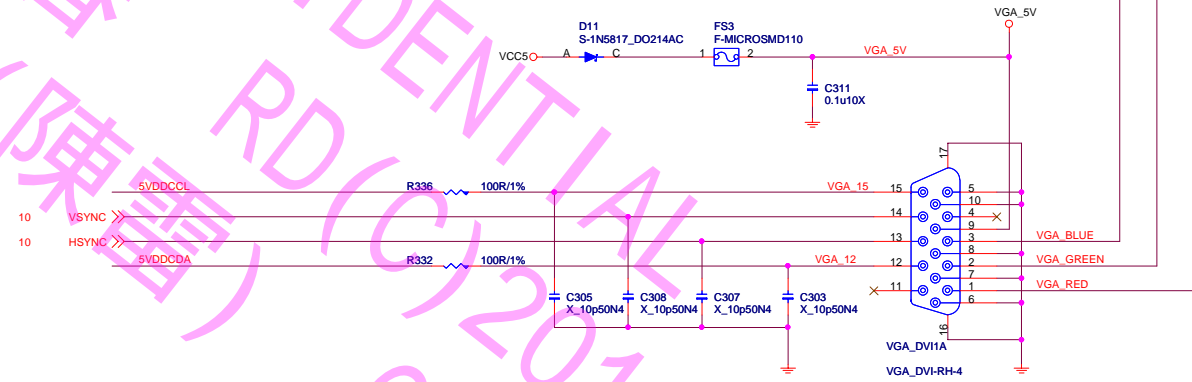
D-Sub

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

Level shift



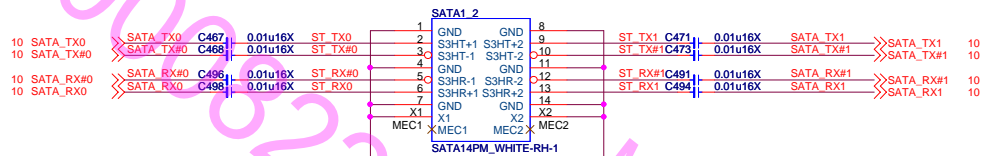
PLACE CLOSE TO VGA CONNECTOR,
WITHIN 750 MIL OF PIN



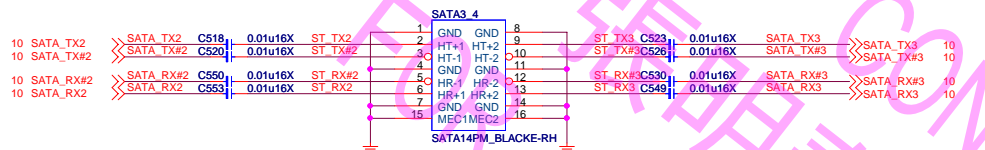
SATA1-2

3.0

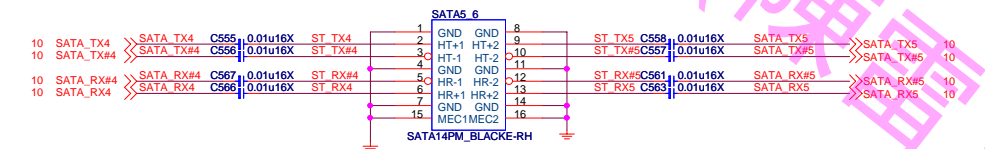
white



SATA3-4



SATA5-6

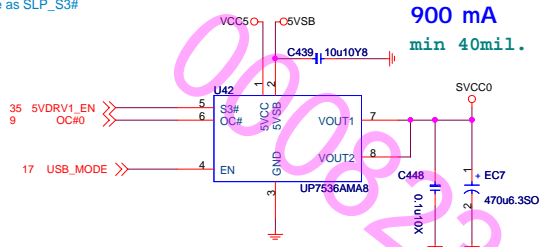


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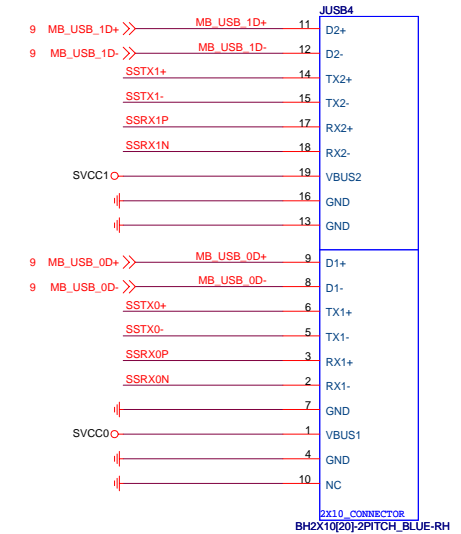
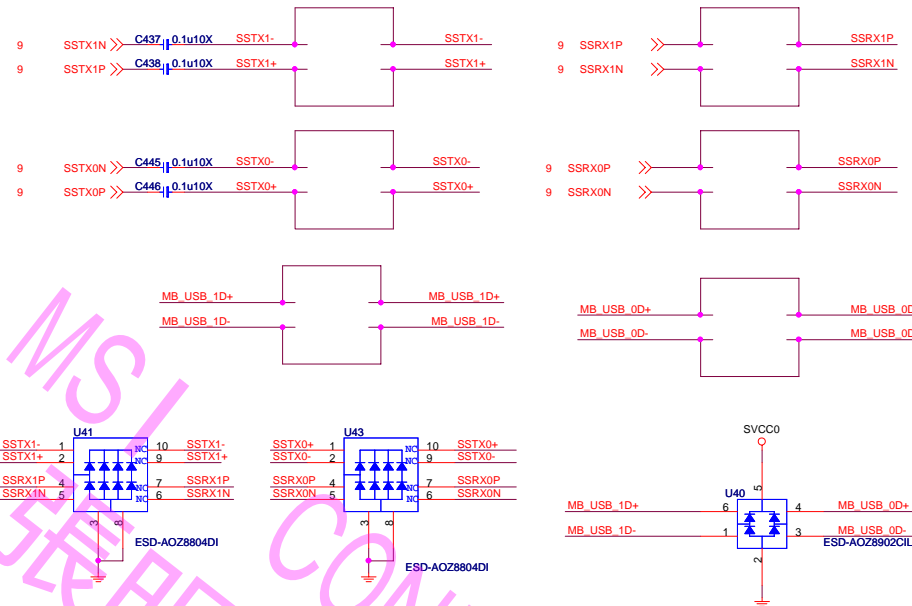
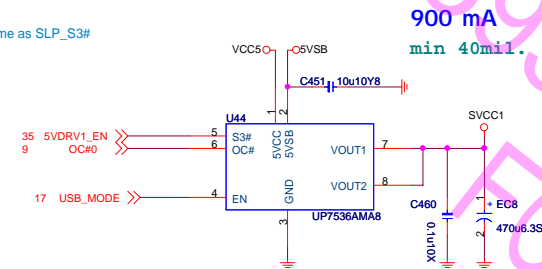
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Size	Document Description	Rev
Custom	SATA Connector	1.0
Date: Thursday, October 20, 2011		Sheet 23 of 41

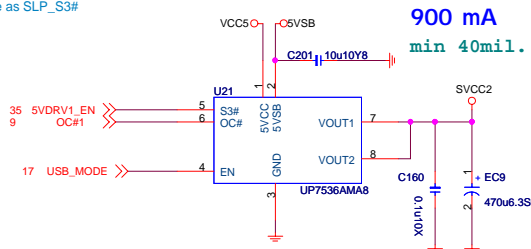
Same as SLP_S3#



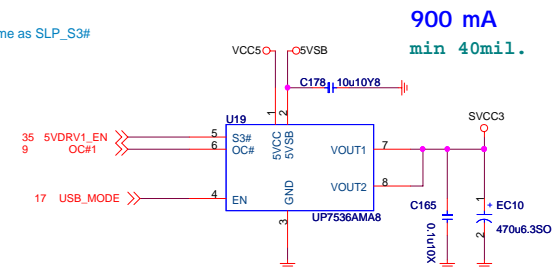
Same as SLP_S3#



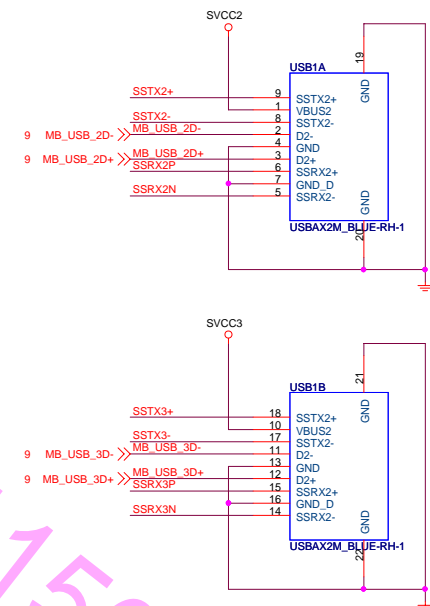
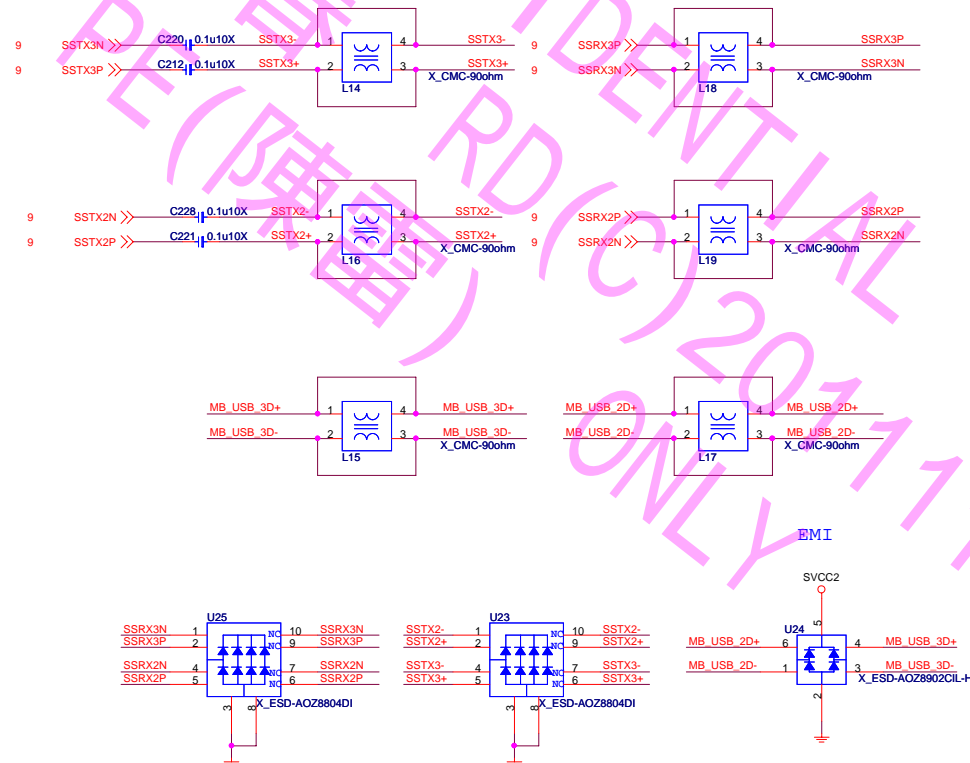
Same as SLP_S3#



Same as SLP_S3#



MODE	G3	S4/S5	S0	S3
EUP Disable	0	0	1	1
EUP Enable	0	0	1	1



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Size Custom	Document Description USB3.0 Connector	Rev 1.0
Date: Thursday, October 20, 2011		Sheet 24 of 41

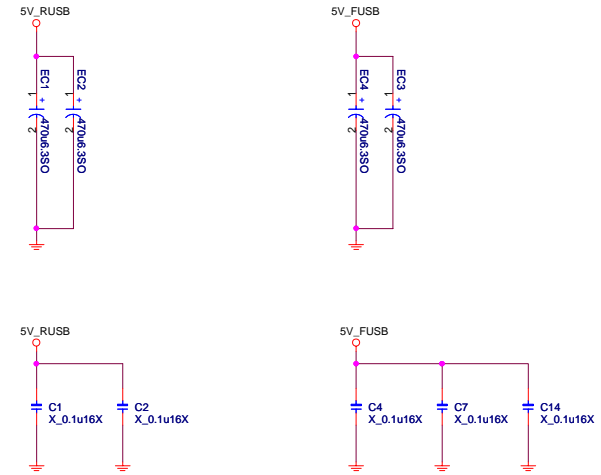
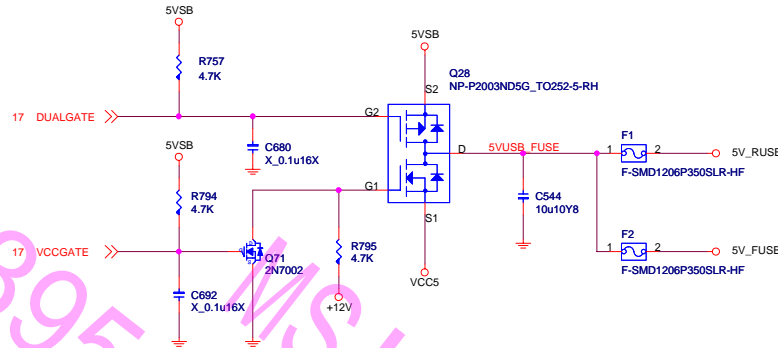
USB2.0/PS2 POWER Control			
MODE	S5	S0	S3
S3P5_Gate#	0/1	1	0
S0P5_Gate#	1	0	1

When PS2 in S5 not support wake , S3P5_Gate# in S5 must setting to High

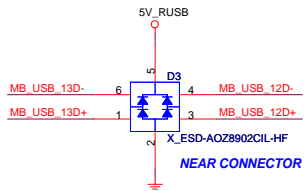
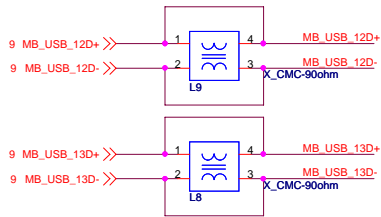
When PS2 in S5 support wake , S3P5_Gate# in S5 must setting to Low

*In S5# (S3P5_Gate# pin status is Tri-state, and can be programmed Low level.

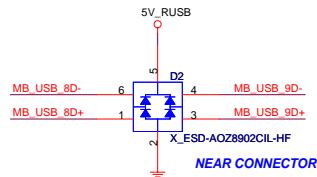
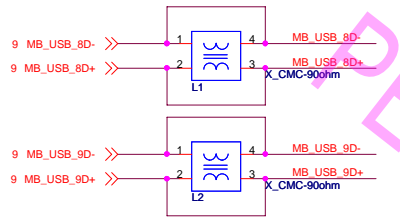
*S3P5_Gate# and S0P5_Gate# can't setting to low together, avoid leakage voltage issue



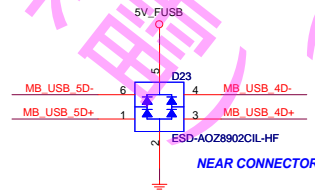
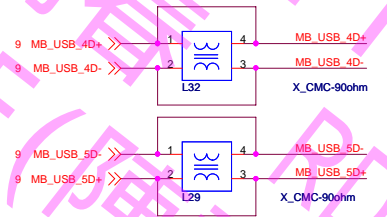
REAR USB PORT 8,9 (With PS2)



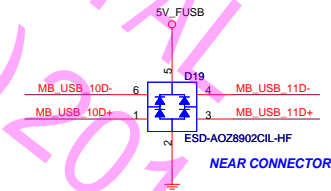
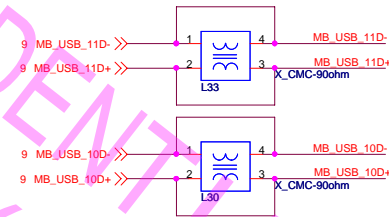
REAR USB PORT 8,9 (With PS2)



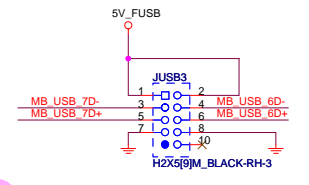
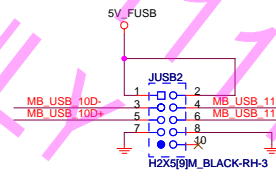
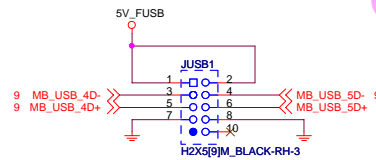
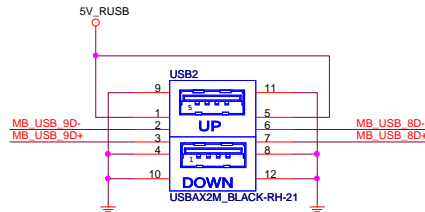
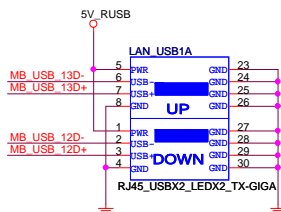
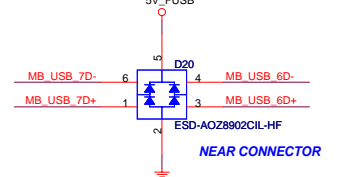
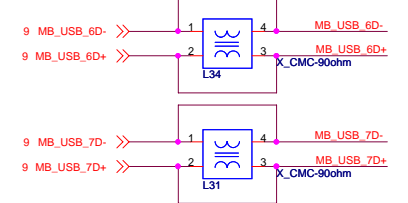
FRONT USB PORT 0,1



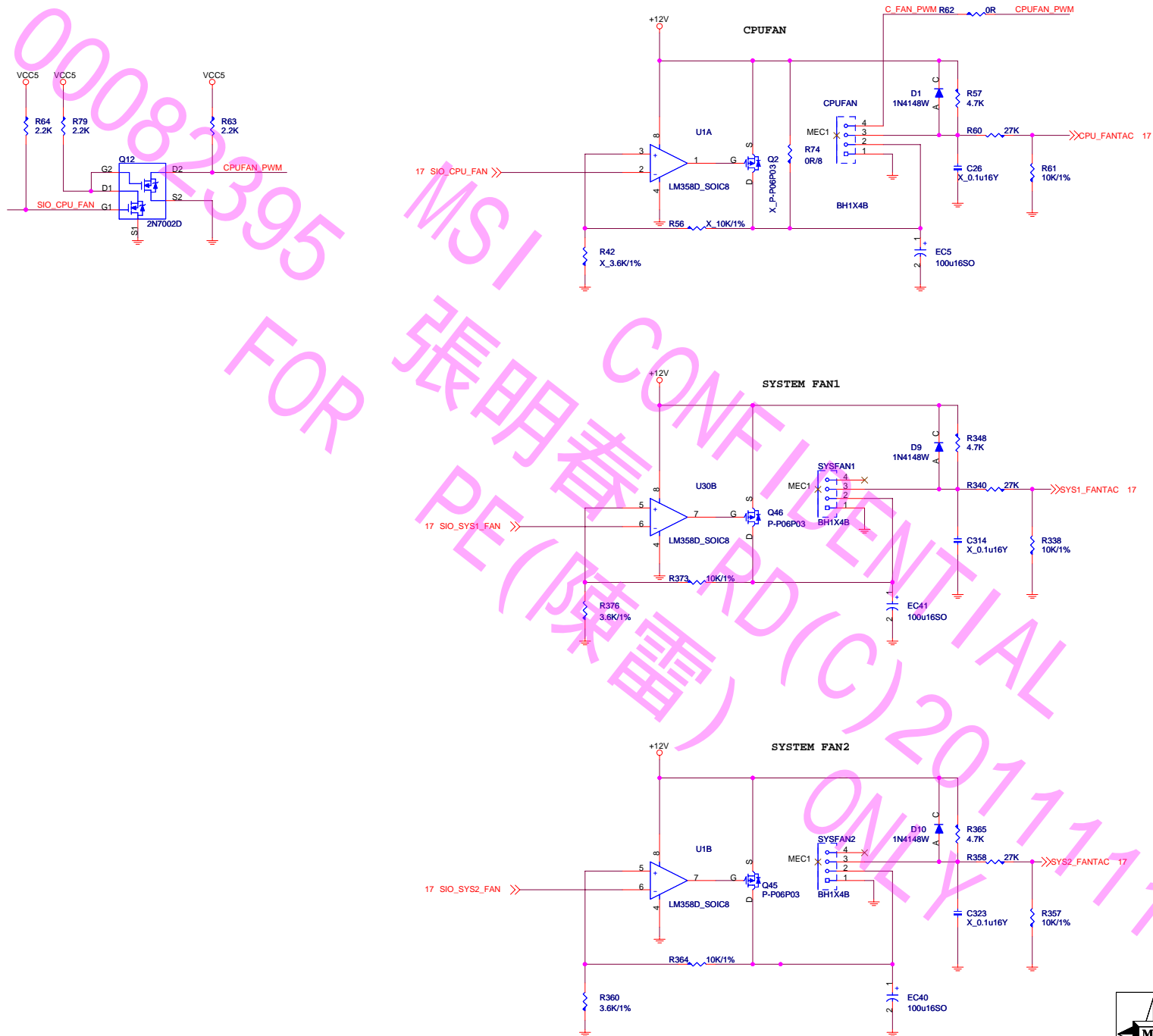
FRONT USB PORT 8,9



FRONT USB PORT 10,11



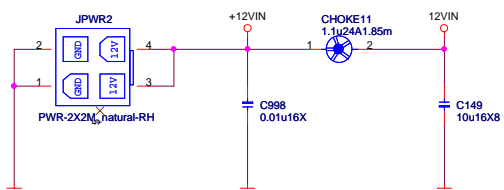
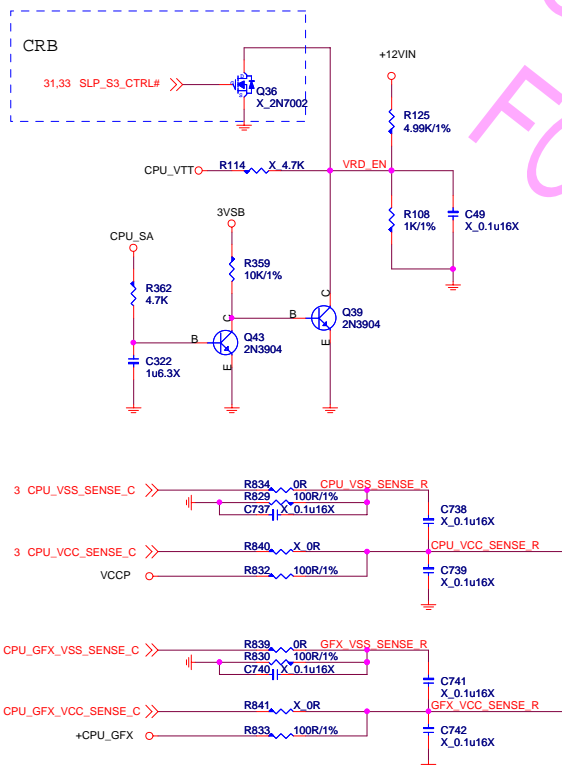
FAN-COUNTROL CIRCUIT



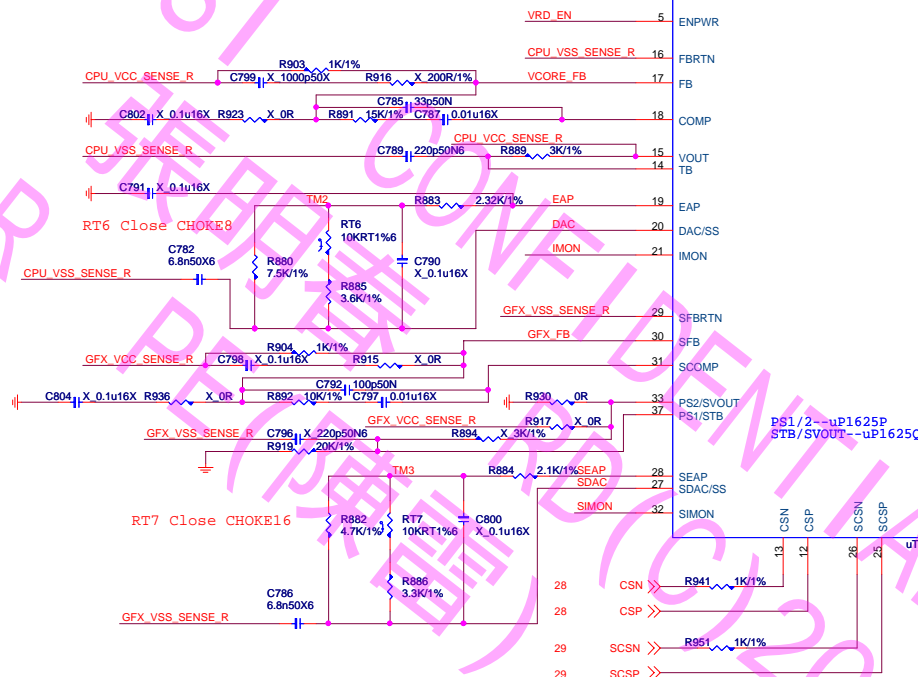
MICRO-STAR INT'L CO.,LTD

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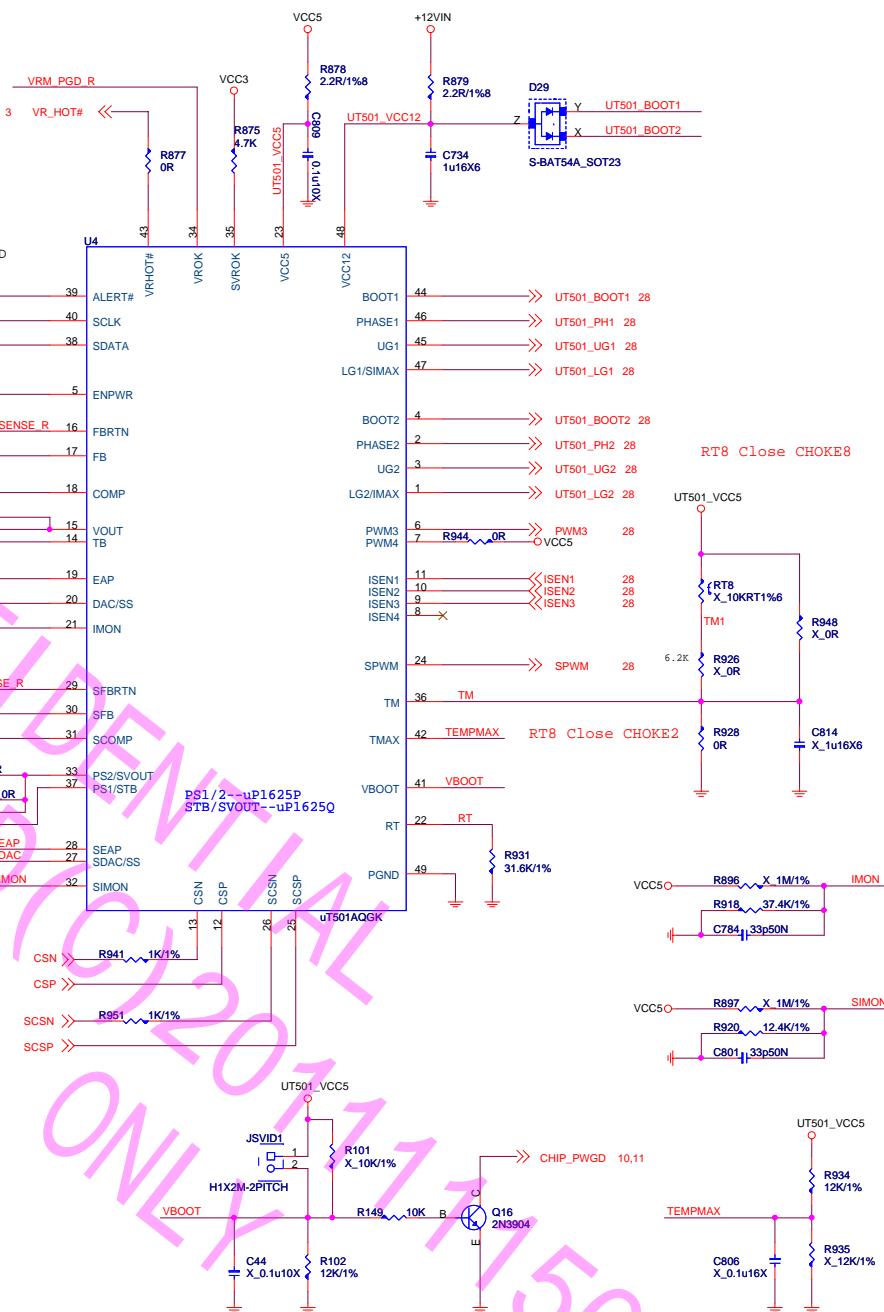
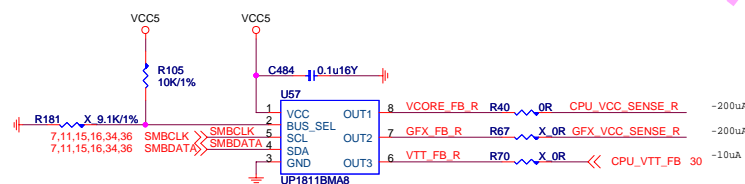
Size	Document Description	Rev
Custom	FAN Control	1.0
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3	VID_ALERT#	>>	VID_ALERT#
3	H_VIDSCLK	<<	H_VIDSCLK
3	H_VIDSOUT	<<	H_VIDSOUT

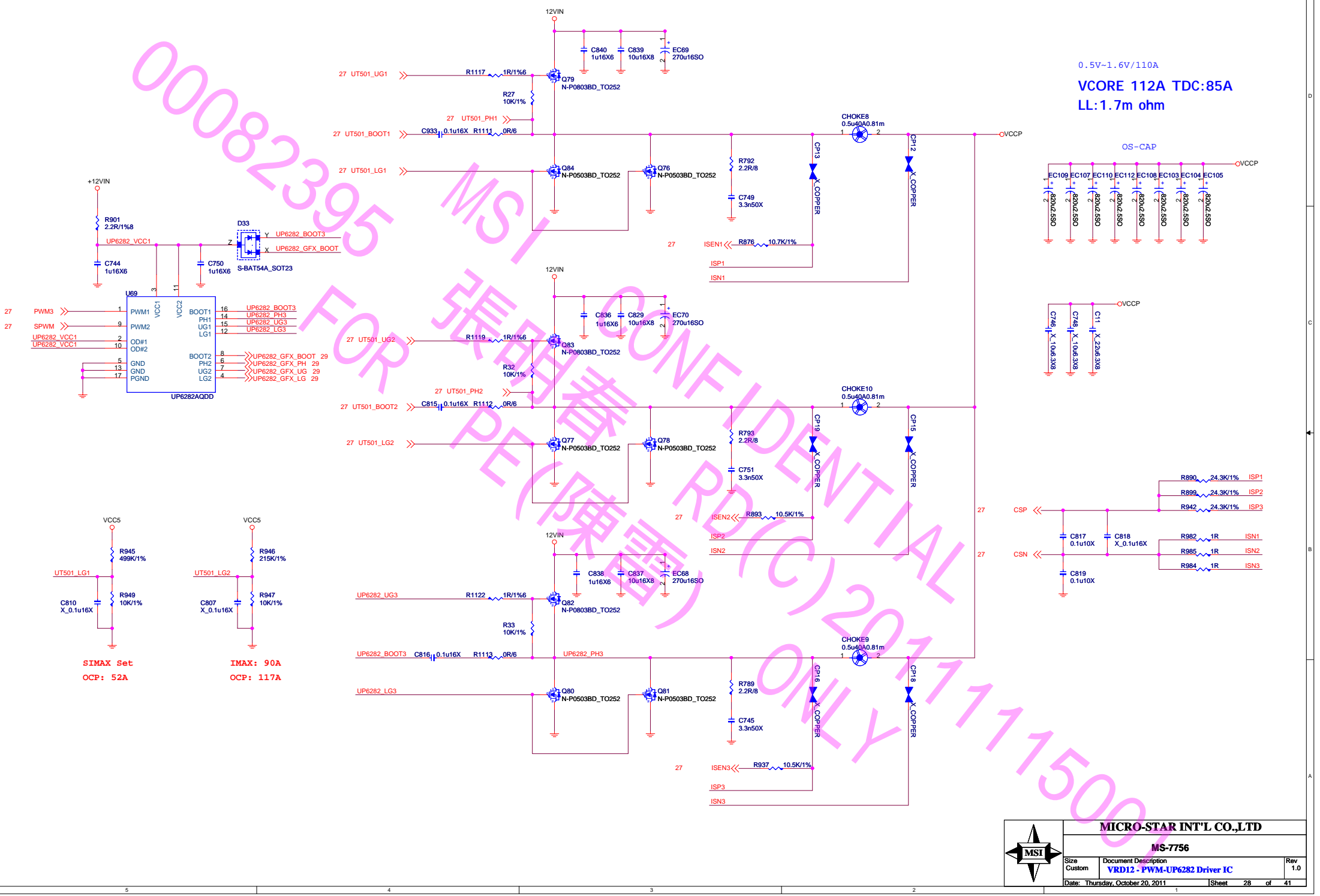


0x20: RH=10K, RL=OPEN						
ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

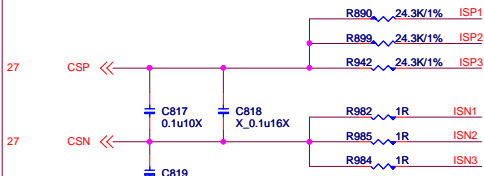
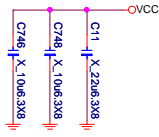
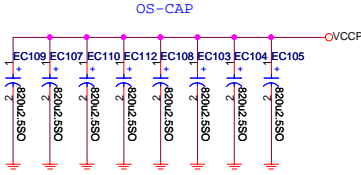


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Size Custom	Document Description VRD12 - PWM-UT501	Rev 1.0
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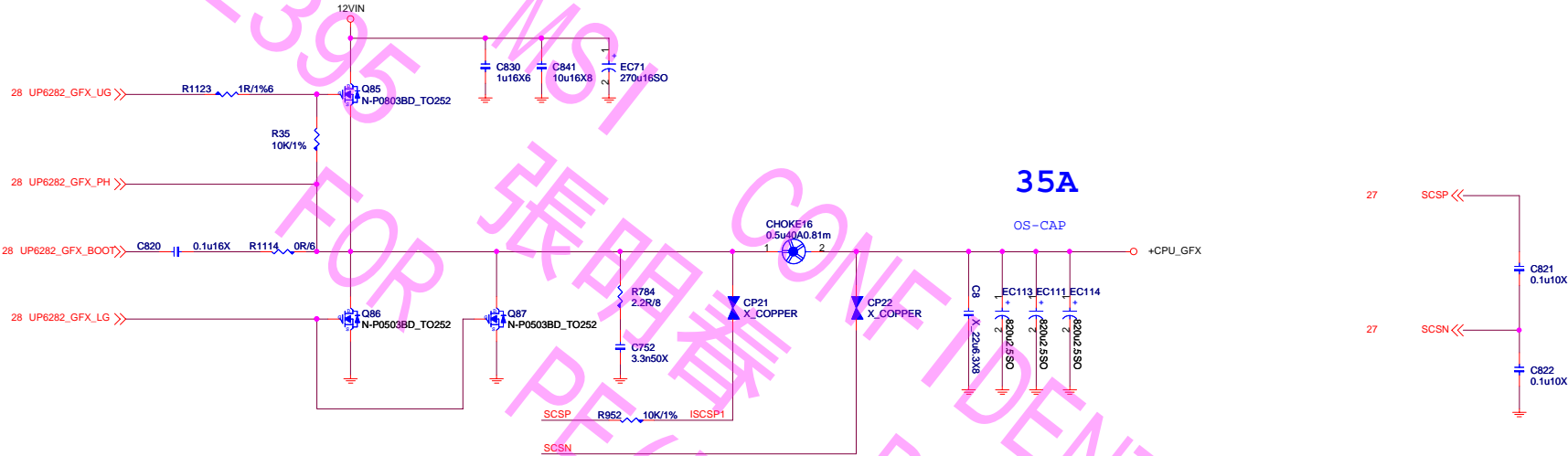


0.5V~1.6V/110A
VCORE 112A TDC:85A
LL:1.7m ohm



CPU_GFX:0.25-1.52

35A FOR CPU

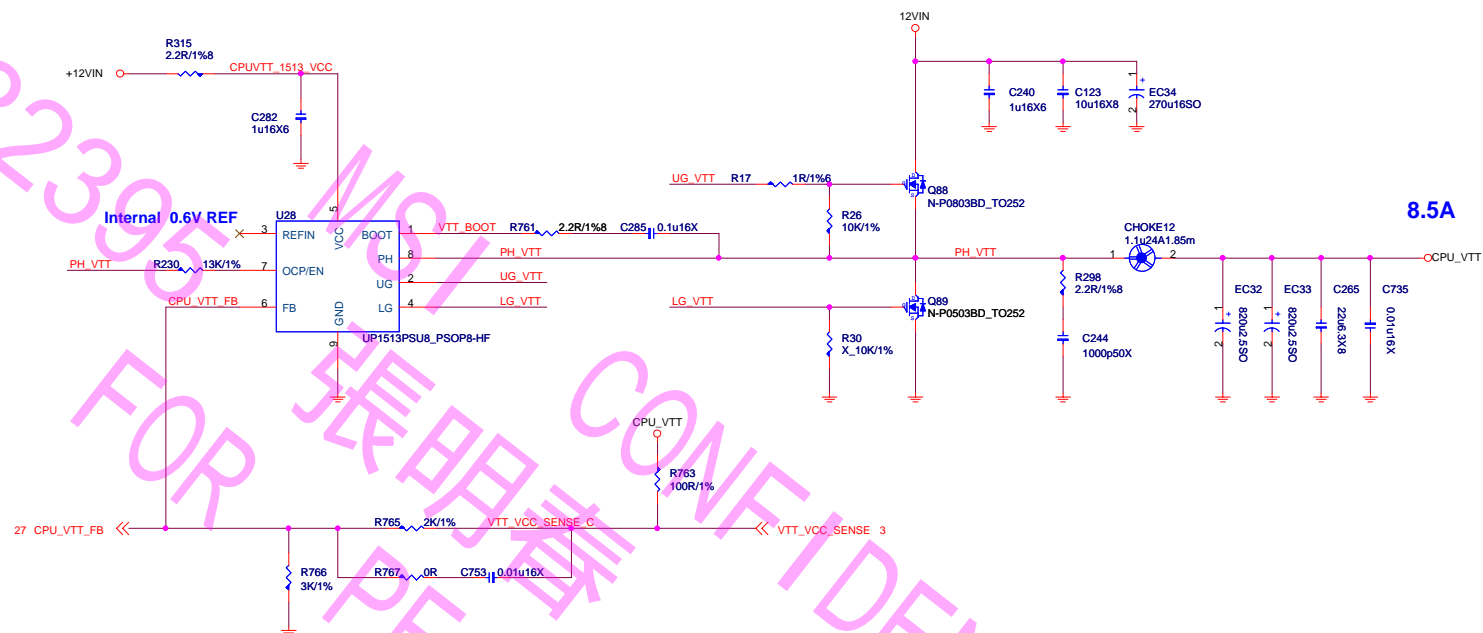


CPU_VTT:1.05/1.00 MAX 17.3A

CPU VTT 8.5A SA Core =8.8A

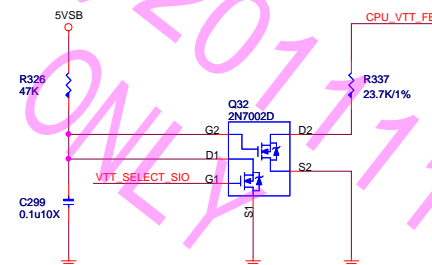
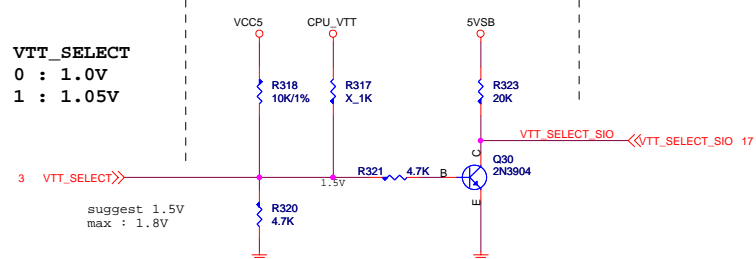
8.5A FOR CPU

$I_{ripple} = 1.92(vtt) + 1.88(sa)$
 $5 * 1 = 5A > 3.8A$



VTT_SELECT	
Low	1.0V
High	1.05V

VTT_SELECT Table	
Low	1.05V
High	1.0V



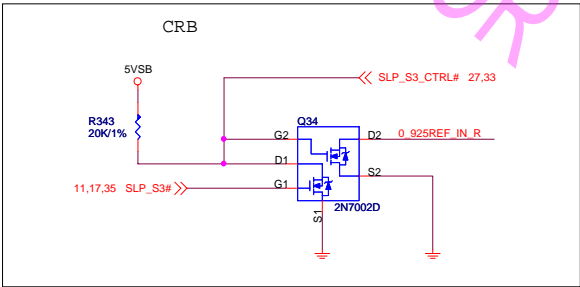
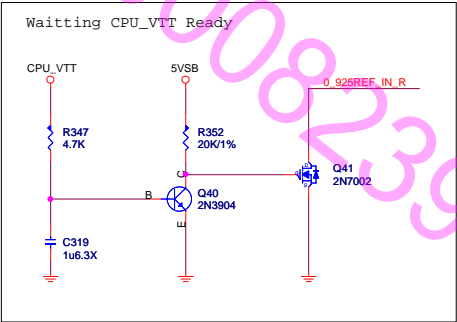
MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	VTT POWER- uP1513- 1Phase MOS	1.0
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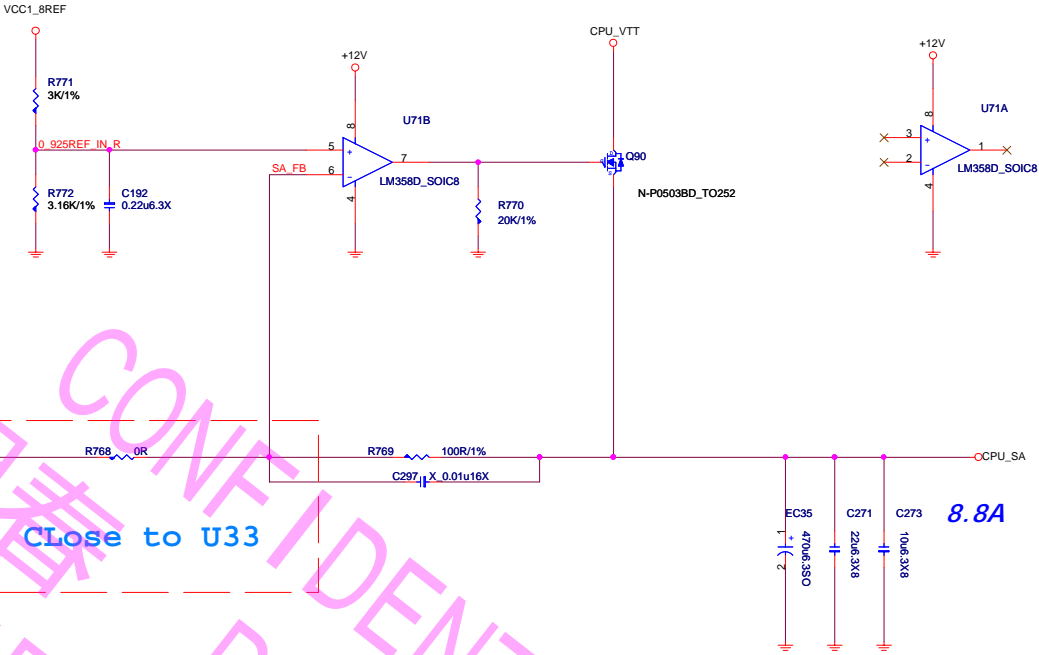
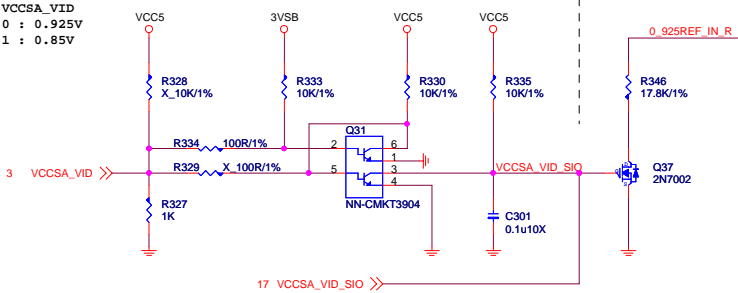
CPU_SA:0.925/0.85

SA Core =8.8A



VCCSA_VID	
Low	0.925V
High	0.85V

VCCSA_VID_SIO Table	
Low	0.925V
High	0.85V



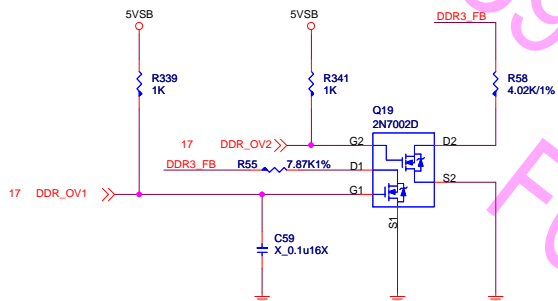
DDR Power:1.5V

DDR3_1.5V 4.75A+15A+1A=20.75A

4.75A FOR CPU
15A FOR 4DIMM
1A FOR DDR VTT

Tripple=8A
 $4.7*2*1=9.4A>8A$

DDR OV



*Default 1.5V

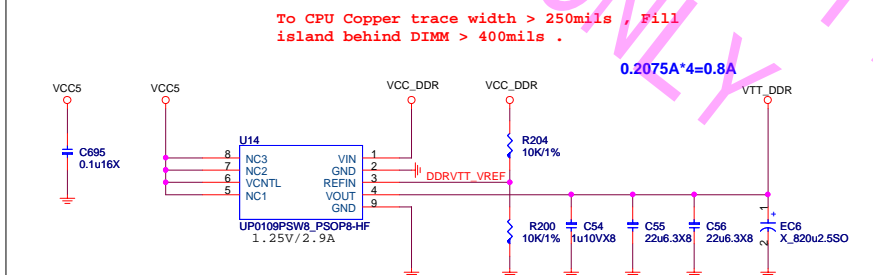
DDR_OV	1.35V	1.5V	1.65V	1.8V
DDR_OV1	Low	High	Low	High
DDR_OV2	Low	Low	High	High

DDR_OV1 = GPIO01(S/IO)

DDR_OV2 = GPIO02(S/IO)

$$((R221/R226)+1)*0.6=1.5V$$

DDR VTT Power



To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

$$0.2075A*4=0.8A$$

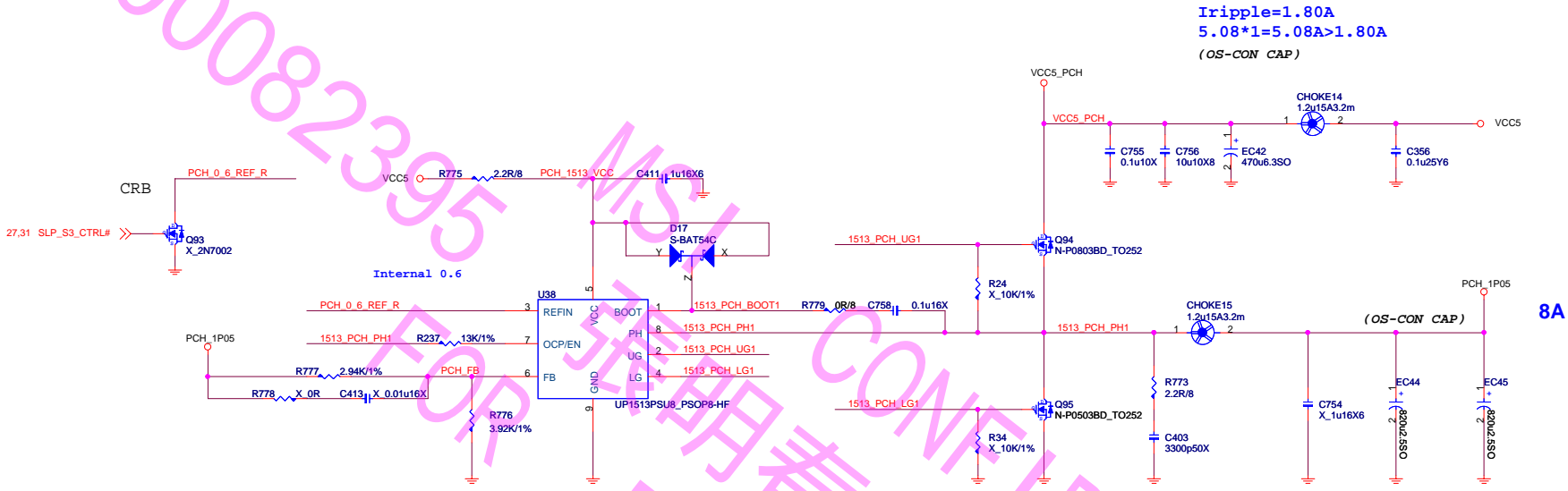


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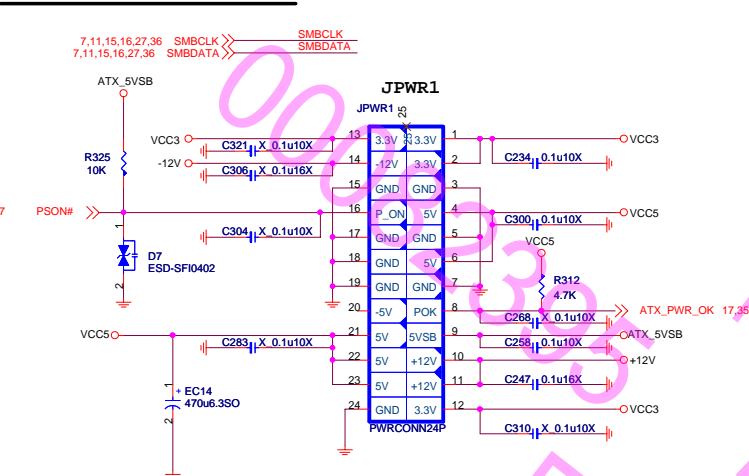
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Size	Document Description	Rev
Custom	DDR Power -UP1513 1-Phase MOS	1.0
Date:	Thursday, October 20, 2011	Sheet 32 of 41

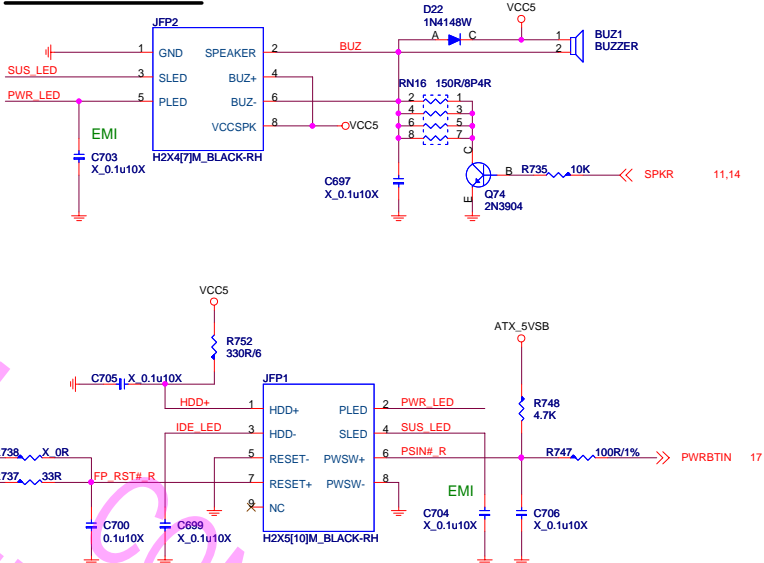
PCH Power:1.05V
PCH Core 6.2A+1.8A=8A
6.2A FOR PCH
1.8A FOR ME CORE



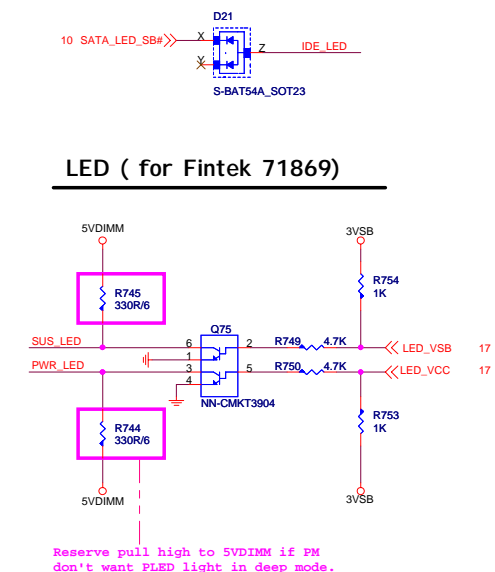
ATX POWER CONNECTOR



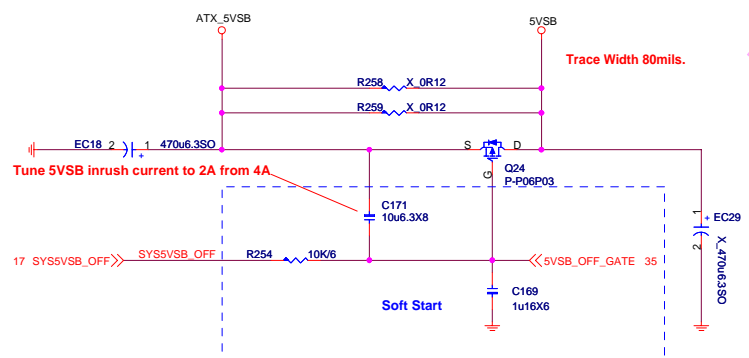
FRONT PANNEL



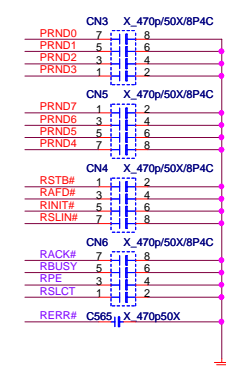
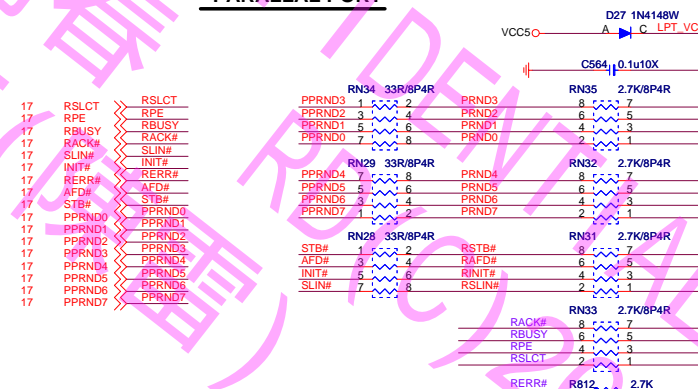
LED (for Fintek 71869)



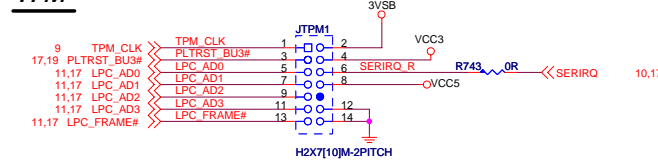
5VSB Power Switch



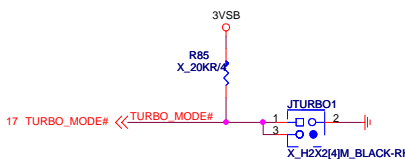
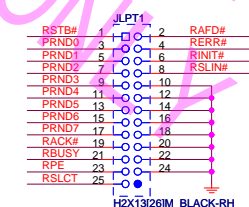
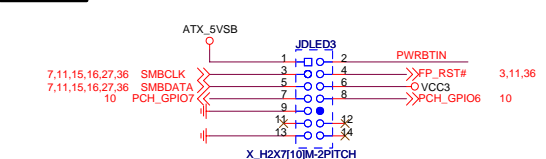
PARALLAL PORT



TPM



Turbo Button

JDLED3

N31-2131151-H06 : 2.0mm
N31-2131131-H06 : 2.54mm



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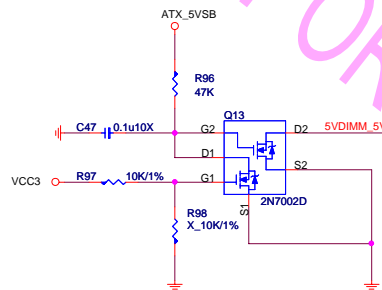
Size Custom	Document Description ATX F_Panel/EMI/TPM	Rev 1.0
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[illegible]

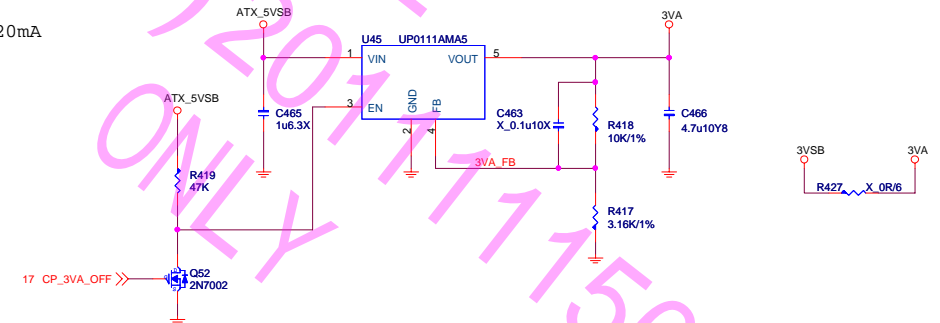
```
7501 Mode
H:Support S0/S3/S5
L:Support S0/S3
```

5VDRV1看VCC5起來6-10ms後起來,因為當初挑power

1.676A



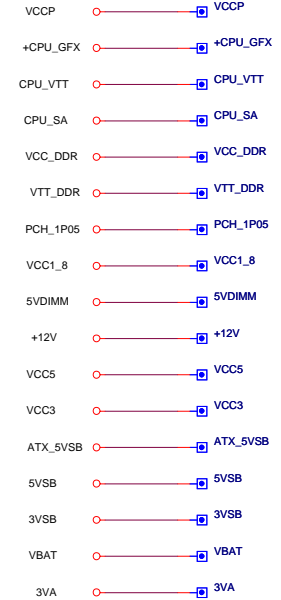
20mA



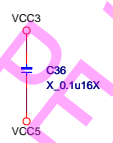
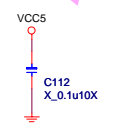
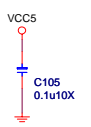
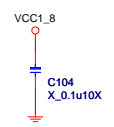
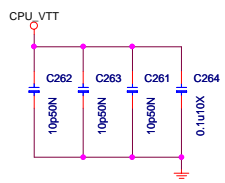
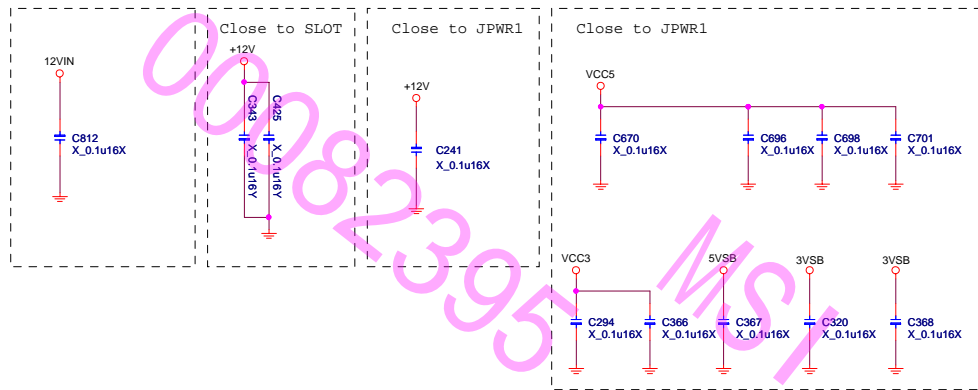
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Voltage test point



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